Universität des Saarlandes
FR 6.2 - Informatik
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Exercise Sheet 8
Computer Architecture II
(Due: Dec 17th, 2013)

Exercise 1: (Memory Management Unit) **(10 Points)**

Figure 13.10 in the draft for the new System Architecture book[1] shows an implementation of a simple memory management unit. The implementation of the *phase* and E signals were given in the lecture. The simulation relation between an ISA configuration c and a hardware configuration h is given as follows.

$$sim(c,h) \equiv h.pc = c.pc \wedge h.gpr = c.gpr \wedge h.spr = c.spr \wedge \forall a \in \mathbb{B}^{30}.\ h.m(a) = c.m_4(a00)$$

Now assume that $sim(c, h^t)$ holds for an ISA configuration c and some implementing hardware state h^t in cycle t, where $h^t.mode[0] = 1$, $h^t.phase = 00$. Prove the following statements:

$$\begin{aligned} ma(h^t) &= ptea(c, c.pc)[31:2] \\ ma(h^{t+1}) &= pma(c, c.pc)[31:2] \\ ma(h^{t+2}) &= ptea(c, ea(c))[31:2] \\ ma(h^{t+3}) &= pma(c, ea(c))[31:2] \end{aligned}$$

Exercise 2: (Page Table Length Exception) **(10 Points)**

Figure 13.11 in *sysbook* depicts the implementation of the page table length exception signal *ptle*. Prove its correctness, i.e.:

$$\langle ptle \rangle \equiv \langle ptl \rangle \leq \langle va \rangle$$

The correctness of the adder and the equality tester can be assumed.

Exercise 3: (Hardware Correctness Proof) **(20 Points)**

In the lecture we have defined the stepping function $t(i)$ for the correctness theorem of the MIPS processor implementation with interrupts and address translation. We assume an ISA computation (c^i) as well as a hardware computation (h^t) and a sequence of hardware external event signals (eev_h^t), where $h^{t+1} = \delta_H(h^t, eev_h^t)$, such that $sim(c^i, h^{t(i)})$ holds for a given i. Now prove the induction step of the MIPS processor implementation correctness theorem:

$$\exists eev_{isa}.\ sim(\delta_{MIPS}(c^i, eev_{isa}), h^{t(i+1)})$$

Missing details of the implementation can be looked up in *sysbook*. The correctness of the regular MIPS implementation without interrupts and address translation may be assumed.

[1] C. Baumann & W. J. Paul & S. Schmaltz, "System Architecture as an Ordinary Engineering Discipline", available on the course's website, a.k.a. "*sysbook*"