Universität des Saarlandes
FR 6.2 - Informatik
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Exercise Sheet 12
Computer Architecture II
(Due: Jan 28th, 2014)

Exercise 1: (Virtual TLB Steps) **(10 Points)**

In the lecture we have defined a Virtual TLB *Xtlb* for $X \in \{I, D\}$ which abstracts from the hardware TLB in the sequential MIPS reference implementation. For the simulation between the virtual and the hardware TLB we have also stated which virutal TLB steps are taken maintain the abstraction. For these steps we can show a lemma, saying that every valid entry of the hardware TLB is contained in the virtual TLB. Prove by induction on cycles t:

$$\forall t, i.\ h^t.tlb_X[i].v \implies h^t.tlb_X[i] \in Xtlb(h^t)$$

Exercise 2: (Core Steps) **(10 Points)**

For the simulation proof between the sequential MIPS hardware and the ISA specification we defined the simulated core actions $a = (core, w_I, w_R)$ containing non-deterministic choices w_I, w_R for the walks that shall be used in address translation. Given that configuration $c^{NE(t)}$ is simulated by hardware state h^t, and a core step a as specified above is executed, prove that for all core steps w_I and w_R are contained in the virtual TLB.

$$\{w_I, w_R\} \subseteq c^{NE(t)}.tlb = Dtlb(h^t) \cup Itlb(h^t)$$

Exercise 3: (MMU Correctness) **(5+5+5+5 Points)**

In the simulation of hardware steps with enabled address translation we have used the following statements.

a) $ue_1^t \wedge mode^t \wedge /malf^t \implies pmaI^{t+1} = pmaI(c, a)$, for $a = (core, w_I^{t+1}, *)$

b) $ue_1^t \implies pff^t = pff(c, a)$, for $a = (core, w_I^{t+1}, *)$

c) $ue_2^t \implies I^{t+1} = I(c, a)$, for $a = (core, w_I^{t+1}, *)$

d) $ue_6^t \wedge l(I^t) \wedge /mca.5.pfls^t \implies lres^{t+1} = lres(c, a)$, for $a = (core, w_I^{t+1}, w_R^{t+1})$

Show that they indeed hold!