Universität des Saarlandes
FR 6.2 - Informatik
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Exercise Sheet 11
Computer Architecture II

(Due: Jan 21th, 2014)

Exercise 1: (TLB Correctness) **(6+6+8 Points)**

In the lecture we have presented an implementation of a translation look-aside buffer as a queue of k registers. However our presentation was incomplete.

a) First, we did not give a formal specification of the TLB component. We can represent the TLB content as a list $tlb \in \mathbb{K}_{walk}^*$ with $|tlb| \leq k$. Specify the outputs *tlbhit* and *tlbwout* as well as the next state tlb' depending on inputs a, *win*, w, *invlpg*, and *flush*!

b) Internally we keep track of the number of entries stored in the TLB via a $k+1$ bit register called *lof* (lowest free line). However it was not shown how this register is updated for the various TLB actions. Moreover we did not take care of the case when the TLB is full and has to drop a walk in order to save a new entry. Here the TLB uses a FIFO eviction policy. Complete the implementation of the TLB!

c) Now the correctness of the TLB implementation shall be proven. Provide a suitable coupling relation and show that the construction implements your specification of the TLB!

Exercise 2: (TLB as RAM) **(10+10 Points)**

The TLB implementation from the lecture is not very energy-efficient, since in the worst case all registers in the entry queue need to be clocked. Alternatively, the TLB can be implemented as a ring buffer using a construction similar to that of a RAM.

a) Provide such an implementation of a TLB!

b) State a coupling relation between your design and the specification from Exercise 1! Prove the correctness of your implementation!