Universität des Saarlandes
FR 6.2 - Informatik
Prof. Dr. W.J. Paul
Dipl.-Ing. Christoph Baumann

Exercise Sheet 9
Computer Architecture II
(Due: Jan 17th, 2012)

Exercise 1: (Cycle Lemma) **(5+5+5 Points)**

In the lecture we proved the following Lemma for the case $\tau_r \leq \tau_s$ with $k \in [1:128]$ when the relative clock drift wrt. τ_{ref} is bounded by $\delta \leq 0.39\%$ in both directions.

- $cy(i+1) \in cy(i) + [0:2]$
- $cy(i+1) \neq cy(i) + 1 \Rightarrow cy(i+1+k) = cy(i+1) + k$

Now prove the Lemma for the other case $\tau_r > \tau_s$! In order to do so follow the steps below! Let $a = cy(i)$ be the first receiver cycle affected by sender edge i.

a) Sketch a timing diagram, where the situation $cy(i+1) = cy(i)$ occurs i.e., the first affected cycle of the next sender edge is the same receiver cycle a. Determine the necessary condition on $e_r(a)$ such that this happens!

b) Prove that when the condition does not hold we have $cy(i+1) = cy(i) + 1$!

c) Show the second part of the Lemma i.e., if the situation $cy(i+1) = cy(i)$ occurs sender and receiver will be in sync for the next k cycles.

Exercise 2: (Estimating Clock Drift) **(5 Points)**

Above we showed that clock synchronization is not necessary for $k \leq 128$ consecutive cycles assuming $\delta \leq 0.39\%$ for the relative clock drift. Estimate the upper bound for k if $\delta \leq 0.15\%$!

Exercise 3: (Majority Voter) **(5+5 Points)**

An n-bit majority voter $n\text{-}maj$ is a circuit with inputs $x \in \mathbb{B}^n$ and output $v \in \mathbb{B}$ such that the voted bit v is 1 if the absolute majority of input bits is 1. Formally it computes the function $v = n\text{-}maj(x[1:n])$ which is defined as follows.

$$n\text{-}may(x[1:n]) = 1 \iff \#\{i \mid x[i] = 1\} \geq \lceil n/2 \rceil$$

a) Construct an n-bit majority voter!

b) Give a correctness proof for your implementation!