Universität des Saarlandes
FR 6.2 - Informatik
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Exercise Sheet 7
Computer Architecture II
(Due: Dec 20th, 2011)

Exercise 1: (3/2-Adder) **(3+5+2 Points)**

An n-3/2-Adder is a circuit with inputs $a, b, c \in \mathbb{B}^n$, $c_{in} \in \mathbb{B}$ and outputs $s \in \mathbb{B}^n$, $t \in \mathbb{B}^{n+1}$ such that the following specification holds:

$$\langle a \rangle + \langle b \rangle + \langle c \rangle + c_{in} = \langle s \rangle + \langle t \rangle$$

a) Construct an n-3/2-Adder!

b) Give a correctness proof for your implementation!

c) Calculate the exact cost and delay of the adder!
Note: The minimal cost and delay for a Full Adder are $C(FA) = 11$ and $D(FA) = 4$.

Exercise 2: (Significand Normalization Shifter) **(10 Points)**

Figure 1 depicts the implementation of the significand normalization shifter in the FPU rounding unit. The significand $f' = f_r/2 > 0$ is put in a cyclical left shifter with shift amount $\langle sh[5:0] \rangle$ where $\sigma = [sh[12:0]] \leq 56$ is the desired left shift distance. Additionally masks $v, w \in \mathbb{B}^{64}$ are computed and anded to the shifter output fs to obtain the normalized significand. In the analysis of the MASK circuit we already derived that $v = \overline{u}$ and $\forall i \in [0:63].\ w_i = u_i \wedge sh[12]$ with:

$$u[63:0] = \begin{cases} 0^{64-\sigma}1^{\sigma} & : \quad 0 \leq \sigma \\ 1^{|\sigma|}0^{64-|\sigma|} & : \quad -63 \leq \sigma \leq -1 \\ 1^{64} & : \quad \sigma < -63 \end{cases}$$

Let $f_n = \langle fn[0].fn[1:127] \rangle$. To be proven:

$$f_n =_p 2^{\sigma} \cdot f'$$

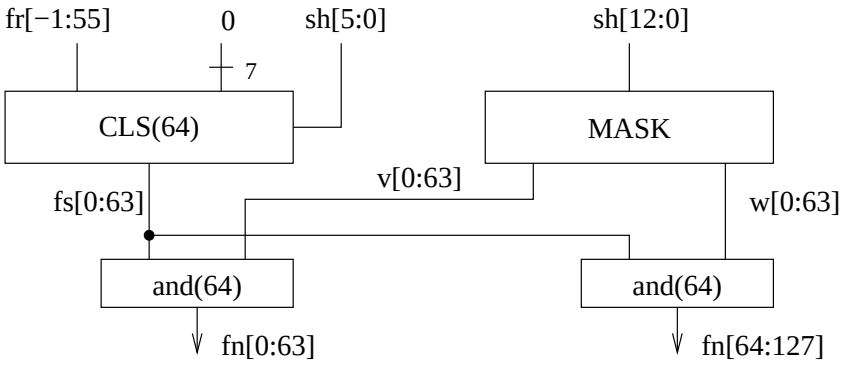

Figure 1: Significand Normalization Shifter

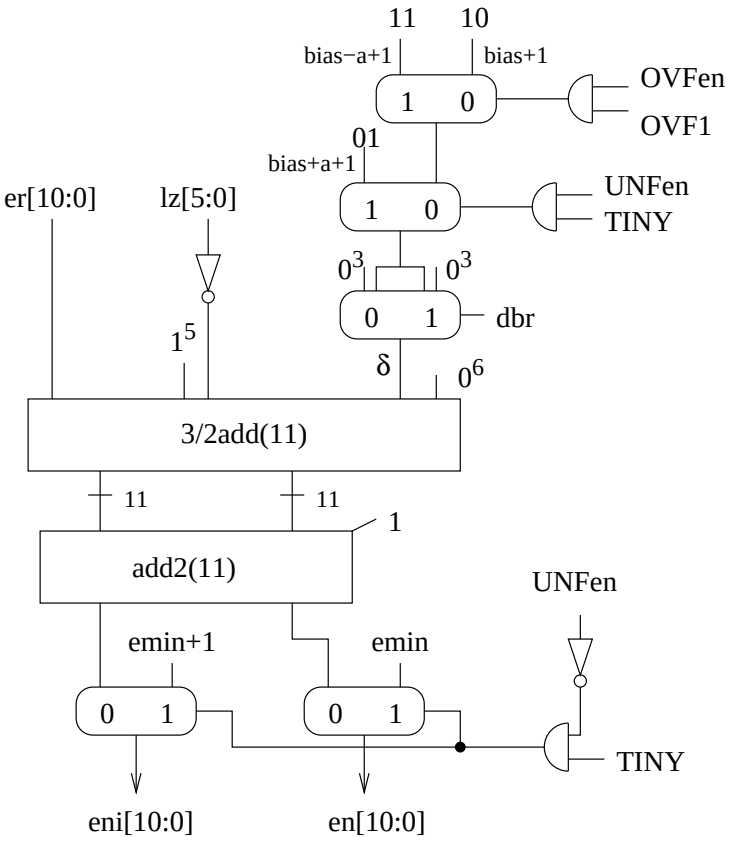

Figure 2: Exponent Normalization Shifter

Exercise 3: (Improved Exponent Normalization Shifter) **(6+2 Points)**

Figure 2 shows the exponent normalization shifter from the FPU rounding unit. One could speed up this circuit by getting rid of the 3/2 Adder. This is done by combining two of the inputs.

a) Show how this can be achieved and that your construction works.

b) How does this modification affect the overall cost and delay of the circuit *ExpNorm*?

Exercise 4: (Previous Slot) **(2 Points)**

In the lecture we defined the notion of schedules for time triggered systems, where time is divided in cycles, slots and rounds. Each round contains ns slots. The next slot after slot s in round r was denoted by the expression $(r, s) + 1$. Give a definition for the previous slot $(r, s) - 1$!