Saarland University
Department 6.2 - Computer Science
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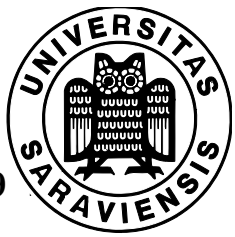

Computer Architecture II - WS 08/09

Exercise Sheet 7 (due: 15.12.08)

Excercise 1: (Improving the Unpacker Circuit) (2 + 2 + 11 points)

In this exercise you should understand and optimize the $UNPACK$ circuit (fig. 8.4, page 355, MP00).

- Explain the function of the incrementers followed by the inverters in this circuit.
- Identify the critical path in the old design of the circuit.
- Optimize the gate delay of the $UNPACK$ circuit approximately by half. To achieve this you have to optimize the delay of the shifter and the interaction of the $LZERO$ and CLS circuits.

  The real delay of $NAND/NOR$ gates counts as 1, whereas AND/OR gates count as 2 gate delays. So, prefer the use of $NAND/NOR$ gates. When optimizing the shifter remember, that you cannot put more than 8 drivers on a bus.

Excercise 2: (Cutting the 3/2 adder in the Exponent Normalizer) (10 + 5 points)

Look at fig. 8.27 in [MP00], page 400: One could speed up this circuit by getting rid of the 3/2 Adder. This is done by combining two of the inputs.

- Show how this can be achieved and that your construction works.
- How does this modification impact the cost and delay of the circuit $ExpNorm$?