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Department 6.2 - Computer Science
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Computer Architecture II - WS 08/09

Exercise Sheet 4 (due: 24.11.08)

Organizational Notes:

- **Students wanting to take part in the examination have to register for it (HISPOS). The HISPOS-registration for the examination is active as from Nov 17th until Dec 05th 2008. Those who have not subscribed to the examination, cannot take part in it or if he/she does, the result cannot be credited.**

Excercise 1: (Sign of Zero) (5 points)

Recall that zero has two representations, i.e. $+0$ and -0. In case of a subtraction, the sign of a zero result depends on the rounding mode:

$$x - x = -x + x = \begin{cases} +0 & if \ \ r_u, r_{ne}, r_z \\ -0 & if \ \ r_d \end{cases}$$

The circuit $ZeroSign$ has three inputs:

- $sa \in \{0,1\}$: the sign of the first operand,
- $s_x = s_a \oplus s'_b 2 \in \{0,1\}$: the effective subtraction signal,
- $RM \in \{0,1\}^2$: rounding mode,

and produces an output $s_s 2 \in \{0,1\}$ which denotes the sign of a zero. In this exercise you have to give the formal specification of the circuit $ZeroSign$ and construct it.

Excercise 2: (Half Decoder) (15 points)
An n-half decoder is a circuit with inputs $x[n-1:0]$ and outputs $Y[2^n-1:0] = 0^{2^n - <x>} 1^{<x>}$, i.e. input x turns on the $< x >$ low order bits of the output.

1. Construct an n-half decoder.
2. Prove the correctness of your construction.