University of the Saarland
Department 6.2 – Informatik
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Computer Architecture II – WS 05/06

(due: Monday, 30.01.2006)

Exercise 1: (Send-Buffer) **(10 points)**

Let:

$D_{in\_p} \in \{0,1\}^{32}$	Data input from processor
$dad \in \{0,1\}^{\lambda+2}$	Device address from processor
$dw \in \{0,1\}$	Device write signal
$SB_{out} \in \{0,1\}^{32}$	Data output to sender
$ads \in \{0,1\}^{\lambda+2}$	Address from sender
$p \in \{0,1\}$	Parity bit from sender

Give a formal specification of a FlexRay Send-buffer.

Exercise 2: (Receive-Buffer) **(15 points)**

Let:

$D_{out\_p} \in \{0,1\}^{32}$	Data output to processor
$dad \in \{0,1\}^{\lambda+2}$	Device address from processor
$D_{in\_r} \in \{0,1\}^{8}$	Data input from receiver
$adr \in \{0,1\}^{\lambda+2}$	Address from receiver
$p \in \{0,1\}$	Parity bit from receiver
$wr \in \{0,1\}$	Write signal from receiver

Give a formal specification of a FlexRay Receive-buffer.