University of the Saarland
Department 6.2 - Informatik
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Computer Architecture II - SS 04

(due: 05.10.2004)

Exercise 1: (Wrapped Exponents) **(5 + 5 points)**

In case a floating point operation produces an overflow or underflow exception the exponent of the result is adjusted and given to the interrupt service routine. In this exercise you have to show that the rounded adjusted result is a normal representable number. Let $\alpha = 3 \cdot 2^{n-2}$. Show for $x = a/b$, a, b representable floating point numbers $\notin \{-\infty, \infty\}$, $b \neq 0$:

1. $OVF(x) \Rightarrow 2^{e_{min}} < |x| \cdot 2^{-\alpha} < X_{max}$
2. $UNF(x) \Rightarrow 2^{e_{min}} < |x| \cdot 2^{\alpha} < X_{max}$

Exercise 2: (Improving the Unpacker Circuit) **(2 + 2 + 11 points)**

In this exercise you should understand and optimize the UNPACK circuit (fig. 8.4, page 355, Müller/Paul: Computer Architecture).

- Explain the function of the incrementers followed by the inverters in this circuit.
- Identify the critical path in the old design of the circuit.
- Optimize the gate delay of the UNPACK circuit approximately by half. To achieve this you have to optimize the delay of the shifter and the interaction of the lzero and CLS circuits as mentioned in the lecture.
  The real delay of NAND/NOR gates counts as 1, whereas AND/OR gates count as 2 gate delays. So, prefer the use of NAND/NOR gates. When optimizing the shifter remember, that you cannot put more than 8 drivers on a bus.

Exercise 3: (End Around Carry Computation) **(2 + 2 points)**

The result of the end around carry adder is computed in the following way:

$$res = \begin{cases} [s] + 1 & \text{if } sub \wedge (a > b) \\ [\bar{s}] & \text{if } sub \wedge (a \leq b) \\ [\text{s}] & \text{if add} \end{cases}$$

In the lecture we already showed the first case where we subtract and $a > b$. Show that the improved adder computes also the correct result in the other two cases.

Exercise 4: (Incorporating the sticky bit into the result of the adder) **(5 points)**

Recall the picture of the Addition/Subtraction Unit from the lecture: Since we optimized the shifter, the sticky bit circuit now lies on the critical path. An optimization would be to compute the sticky bit parallel to the addition. Find a solution to integrate the sticky bit after the addition. Show that your solution gives the correct result.

Exercise 5: (Carry Lookahead Compound Adder) **(4 points)**

Complete the construction of the Carry Lookahead Compound Adder from the lecture.