Saarland University
Department 6.2 - Computer Science
Prof. Dr. W. J. Paul
Geng Chen

Multicore System Architecture - WS15/16

Exercise Sheet 9 (due: 15.1.2016)

Tutor: _____

Name, Matr. Number: _____

Exercise 1: (4)

In the lecture, we pipelined the *nextpc*, *pc* and *dpc* such that $X \in \{nextpc, pc, dpc\}$. $X.k$ belongs to the instruction in stage k.

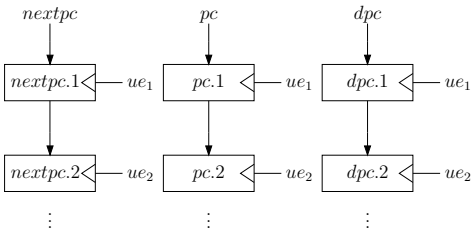

Figure 1: PC pipeline

What is stored in $X.1$ when $full_1^t \wedge ue_1^t$? (1 point) The *epc* and *edpc* are updated when *jisr* as follows:

$$epc = \begin{cases} nextpc.4 & cont.4 \\ pc.4 & otherwise \end{cases}$$

$$edpc = \begin{cases} pc.4 & cont.4 \\ dpc.4 & otherwise \end{cases}$$

Here, we simplify the problem by assuming no move instructions exist in the interrupt service routine. After handling the interrupt we have *eret*, which updates the *epc* and *edpc*. The *eret* instruction will restore the *pc* and *dpc* and drain the pipe as well. In this case, we have $full_1 = 0$. Since we defined

$$ima_\pi = \begin{cases} dpc_\pi.l & full_1 = 0 \\ pc_\pi.l & full_1 = 1 \end{cases}$$

the machine will fetch from *dpc* which is restored from the *edpc*. The value of *edpc* is the instruction address of the interrupted instruction if it is a continue interrupt, otherwise is the instruction address of the instruction before the interrupted one. We fix this bug by dropping the $X.1$ and setting $X.2in = X$. Prove that: $X_\pi^t = X_\sigma^{I(2,t)-1}$ (3 points) (Hint: $X.k$ is an invisible register.)

Exercise 2: (5)

In our current construction, the TLB might drop walks even though there are still "empty" cache lines due to *invlpgs*. This is not very efficient. Improve the construction such that if the TLB is not full then valid walks will not be overwritten. Bonus: Change the replacement strategy into LRU (least recently used) (10 bonus points).