Saarland University
Department 6.2 - Computer Science
Prof. Dr. W. J. Paul
Geng Chen

Multicore System Architecture - WS15/16

Exercise Sheet 8 and Christmas gifts(due: 8.1.2016)

Important:

- Each week on Friday one exercise sheet will be released. The solutions should be handed in before or after the next Friday lecture if not stated otherwise. For the admission to the exam you will need at least 50% of the points of the exercises.
- Tutorials: Group A: Wednesday 12:00 - 14:00 (Room 328, E 1 3, Tutor: Jonas Donia) and Group B: Tuesday 10:00 - 12:00 (Room 328, E 1 3, Tutor: Shahd Zahran)
- You are allowed to solve the exercise sheets in groups. Everybody who has his or her name on the solution must be able to present it in the tutorials. Everybody must present the solution of at least two exercises.
- Please, register for the lecture at the lecture's webpage until Nov 13th, 2015!
  http://www-wjp.cs.uni-saarland.de/lehre/vorlesung/rechnerarchitektur/ws15/anmeldung.php
  Also do not forget to register for the exam in the HISPOS system!
- The oral exam will take place in February. An exact date will be decided upon in class.

Tutor: _____

Name, Matr. Number: _____

Exercise 1: **(4)**

In the lecture, we defined the sets

$$A = \{acc(2q+1,k) \in E(t) : q \in [0:p-1] \wedge \neg acc(2q+1,k).f\}$$

and

$$B = \{dacc(q, I(q,4,t)) : q \in PS(t) \wedge \neg void(dacc(q; I(q,4,t)))\}$$

Prove $A = B$.

Exercise 2: **(2)**

Specify the clock enable signal $sprce[i]$ for the SPR. (Hint: each pipelined signal X is written as $X.k$ and do not forget the clock enable signal for $emode$)

Exercise 3: **(2)**

In the lecture, we had a argument on the input of eca. Explain the reason why do we use $mca.4in[31:1] \circ reset$ as the input of eca.

The exercises below are gifts for Christmas. All the points below are bonus points.

Exercise 4: **(6)**

Usually one would mask external interrupts (setting $SR[1] = 0$) during the execution of $eret$ instructions.

1. Suppose we don't do this. Is ISA still correctly simulated by our pipelined hardware or not?

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2. Explain why? Hint: will the external interrupt under consideration be 'cont' or 'repeat'?
3. at which place does this concern the formal correctness proof?

Exercise 5: **(8)**

Forwarding of *epc* and *edpc* for pipe draining instructions was done in order to minimize changes in the correctness proof of the machine, but intuitively it should not be necessary.

1. modify the hardware in this sense by eliminating these forwarding circuits *and* postponing the update of *pc* and *dpc* for *eret* instructions.
2. prove the correctness of this construction in the absence of interrupts. Hint: you have to adjust the scheduling functions and/or the induction hypothesis to reflect the delayed update of the program counters.
3. now consider interrupts too in the correctness proof.

This is not an easy exercise.

Exercise 6: **(8)**

Using speculative execution we can drop the software condition for self modifying code. Normal execution speculates that instructions are not written (in the memory stage) after they have passed the fetch stage.

1. construct hardware which dedetcts the corresponding 'misspeculation on fetch'. Hint: the pipelined PCs and dpc's should help.
2. adjust stall engine and the inputs to the program counters such that the rollback can be implemented. Hint: in which stages can the modified instruction be?
3. prove that this works in the absence of interrupts.
4. now consider in the correctness proof interrupts too.

This is not an easy exercise.