Saarland University
Department 6.2 - Computer Science
Prof. Dr. W. J. Paul
Geng Chen

Multicore System Architecture - WS15/16

Exercise Sheet 5 (due: Nov 27, 2015)

Important:

- Each week on Friday one exercise sheet will be released. The solutions should be handed in before or after the next Friday lecture if not stated otherwise. For the admission to the exam you will need at least 50% of the points of the exercises.
- Tutorials: Group A: Wednesday 12:00 - 14:00 (Room 328, E 1 3, Tutor: Jonas Donia) and Group B: Tuesday 10:00 - 12:00 (Room 328, E 1 3, Tutor: Shahd Zahran)
- You are allowed to solve the exercise sheets in groups. Everybody who has his or her name on the solution must be able to present it in the tutorials. Everybody must present the solution of at least two exercises.
- Please, register for the lecture at the lecture's webpage until Nov 13th, 2015!
  http://www-wjp.cs.uni-saarland.de/lehre/vorlesung/rechnerarchitektur/ws15/anmeldung.php
  Also do not forget to register for the exam in the HISPOS system!
- The oral exam will take place in February. An exact date will be decided upon in class.

Tutor: _____

Name, Matr. Number: _____

In the following series of exercises show how to provide different memeory modes in a multi core machine. The memory mode used so far is called *writeback mode*. We wish to provide a second memory mode called *write through* where

- reads are cacheable.
- a write hit updates the line and the main memory.
- a write miss does not allocate a line.

The same line can be accessed at different ports with different modes. The mode, in which a line was accessed last is *not* maintained in the cache state of lines.

Accesses *acc* are provided with a new component $acc.wt \in \mathbb{B}$ indicating that the access is performed in write through mode. This bit has only an effect for writes.

Exercise 1: **(4)**

Modify the protocol tables. For this purpose replace in the table for master transitions columns *write* and *cas+* by $write, /wt$, $write, wt$, $cas+, /wt$ and $cas+, wt$. Hints:

- Use the protocol signal Ca in the sense 'Intend to run the cache coherence protocol', i.e. also on write misses in write through mode.
- activate in write through mode a master control signal wt. We do not use it in the tables. It is used later to keep control automata in sync.

Exercise 2: **(2)**

Translating tables to switching functions (sec. 8.3.3 of *A Pipelined Multi-core MIPS Machine*[1]).

[1] http://www-wjp.cs.uni-saarland.de/lehre/vorlesung/rechnerarchitektur/ws15/books/multicorebook.pdf

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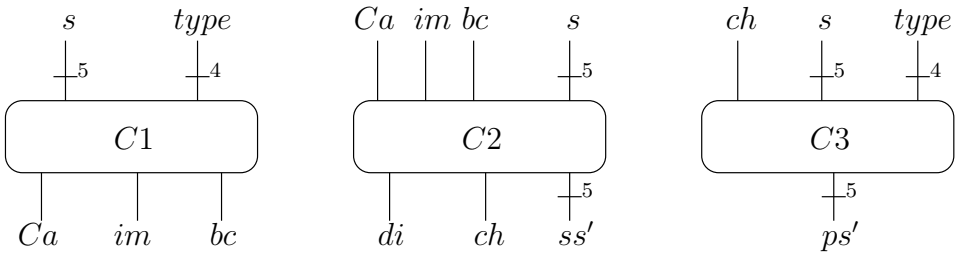
1. which of the circuits C1, C2, C3 deoend on signal wt?
2. redraw the following figure.



Exercise 3: **(4)**

Adjust the algebraic specification of the atomic protocol (sec. 8.3.4 of *A Pipelined Multi-core MIPS Machine*).

Hints:

- writes in write through mode are not local.
- the update of memory in write through mode is similar to a flush.

Exercise 4: **(10)**

Prove that the new columns in the master state transition table in Exercise 1 maintains the state invariants.