Saarland University
Department 6.2 - Computer Science
Prof. Dr. W. J. Paul
Geng Chen

Multicore System Architecture - WS15/16

Exercise Sheet 3 (due: Nov 13, 2015)

Important:

- Each week on Friday one exercise sheet will be released. The solutions should be handed in before or after the next Friday lecture if not stated otherwise. For the admission to the exam you will need at least 50% of the points of the exercises.
- Tutorials: Group A: Wednesday 12:00 - 14:00 (Room 328, E 1 3, Tutor: Jonas Donia) and Group B: Tuesday 10:00 - 12:00 (Room 328, E 1 3, Tutor: Shahd Zahran)
- You are allowed to solve the exercise sheets in groups. Everybody who has his or her name on the solution must be able to present it in the tutorials. Everybody must present the solution of at least two exercises.
- Please, register for the lecture at the lecture's webpage until Nov 13th, 2015!
  http://www-wjp.cs.uni-saarland.de/lehre/vorlesung/rechnerarchitektur/ws15/anmeldung.php
  Also do not forget to register for the exam in the HISPOS system!
- The oral exam will take place in February. An exact date will be decided upon in class.

Tutor: _____

Name, Matr. Number: _____

Exercise 1: (4)

In the lecture, we introduce an implementation of hardware queue as following:

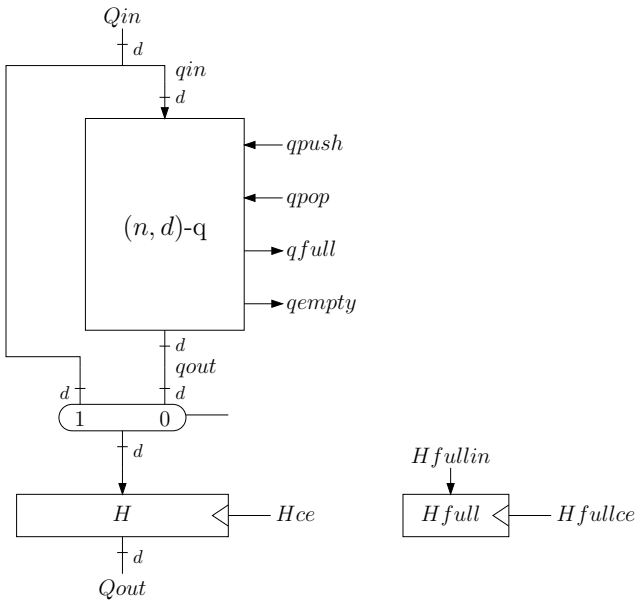

Figure 1: improved hardware queue

1. Choose the correct signal for the multiplexer to complete the implementation. (1 point)
2. Explain the advantage of introducing the auxiliary register H. (1 point)

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3. Assume we have three registers: hp stores the value of the head pointer, tp stores the value of the tail pointer and L stores the length. Implement the (n, d)-q with a 2 ports (n, d)-RAM (in which Sa is the read address and Sb is the write address) and these three registers. (2 points)

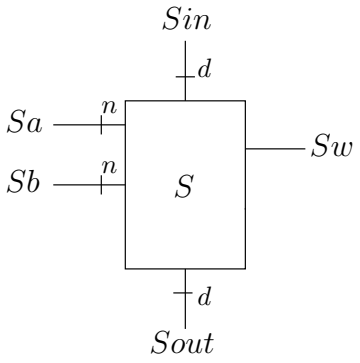

Figure 2: 2-port ram

Exercise 2: **(4)**

In this exercise, we need to implement a (n, r, a)-RAM-ROM

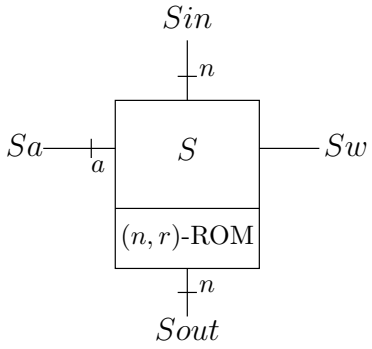

Figure 3: (n, r, a)-RAM-ROM

which satisfies the following specification.

$$S'(x) = \begin{cases} S^0(x) & x[a-1:r] = 0^{a-r} \\ Sin & x = Sa \wedge Sw \wedge x[a-1:r] \neq 0^{a-r} \\ S(x) & \text{otherwise.} \end{cases}$$

Implement the (n, r, a)-RAM-ROM and prove the correctness of your implementation.

Exercise 3: **(7)**

In this exercise we establish correctness of the instruction fetch. Recall the instruction memory environment from the lecture.

1. Assume $sim(c, h)$ and show that the hardware has fetched the correct instruction, i.e.

$$I(h) = I(c) \qquad \text{(3 points)}$$

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2. Explain in words where are you using the alignment in the proof. (2 point)
3. Explain in words why it is important to have a ROM portion in the memory. (2 point)

Exercise 4: **(6)**

In this exercise we establish correctness of the next pc computation. Recall the next pc environment from the lecture.

1. Assume $sim(c, h)$ and show the following statements:

$$\begin{aligned} pcinc(h) &= c.pc +_{32} 4_{32} \\ btarget(h) &= btarget(c) \\ jbtaken(h) &\equiv jbtaken(c) \end{aligned}$$

   For the first one, stress the place where the alignment is required (3 points).

2. Conclude that the pc component of the hardware is updated correctly, i.e.

$$sim(c, h) \rightarrow h'.pc = c'.pc \qquad \text{(3 points)}$$

Exercise 5: **(2)**

Describe in a pipelined machine what is a delay slot and why do we need it.