Saarland University
Department 6.2 - Computer Science
Prof. Dr. W. J. Paul
Geng Chen

Multicore System Architecture - WS15/16

Exercise Sheet 2 (due: Nov 6, 2015)

Important:

- Each week on Friday one exercise sheet will be released. The solutions should be handed in before or after the next Friday lecture if not stated otherwise. For the admission to the exam you will need at least 50% of the points of the exercises.
- Tutorials: Group A: Wednesday 12:00 - 14:00 (Room 328, E 1 3, Tutor: Jonas Donia) and Group B: Tuesday 10:00 - 12:00 (Room 328, E 1 3, Tutor: Shahd Zahran)
- You are allowed to solve the exercise sheets in groups. Everybody who has his or her name on the solution must be able to present it in the tutorials. Everybody must present the solution of at least two exercises.
- Please, register for the lecture at the lecture's webpage until Nov 13th, 2015!
  http://www-wjp.cs.uni-saarland.de/lehre/vorlesung/rechnerarchitektur/ws15/anmeldung.php
  Also do not forget to register for the exam in the HISPOS system!
- The oral exam will take place in February. An exact date will be decided upon in class.

Tutor: _____

Name, Matr. Number: _____

Exercise 1: (6)

In the lecture, we introduced the carry-look-ahead adder (CLA) which has a linear cost and logarithmic delay. The CLA needs the parallel prefix circuit (PP) to compute the generate bits and the propagation bits. The generate bits and propagation bits from index i to index j are defined by the following functions:

$$p_{i,j}(a,b) \equiv \langle a[i:j]\rangle + \langle b[i:j]\rangle = \langle 1^{i-j+1}\rangle$$

$$g_{i,j}(a,b) \equiv \begin{cases} \langle a[i:j]\rangle + \langle b[i:j]\rangle \geq \langle 10^{i-j+1}\rangle & j > 0 \\ \langle a[i:j]\rangle + \langle b[i:j]\rangle + c_0 \geq \langle 10^{i-j+1}\rangle & j = 0 \end{cases}$$

For $i = j$.

$$p_i(a,b) \equiv p_{i,i}(a,b) = a_i \oplus b_i$$

$$g_i(a,b) \equiv g_{i,i}(a,b) = \begin{cases} a_i \wedge b_i & i > 0 \\ a_0 \wedge b_0 \vee a_0 \wedge c_0 \vee b_0 \wedge c_0 & i = 0 \end{cases}$$

1. Knowing

$$\begin{array}{ll} p_{i,k+1}(a,b) & p_{k,j}(a,b) \\ g_{i,k+1}(a,b) & g_{k,j}(a,b) \end{array}$$

   show the computation of $p_{i,j}(a,b)$ and $g_{i,j}(a,b)$ when $i \neq j$ and construct a circuit to implement the computation. (2 points)

2. The PP circuit only works for associative operations. Let $\circ$ be the operation specified by the above functions. Show that $\circ$ is an associative operation, i.e. for all i let $g_i \equiv g_i(a,b)$ and $p_i \equiv p_i(a,b)$ then we have: (2 points)

$$(g_1,p_1) \circ ((g_2,p_2) \circ (g_3,p_3)) = ((g_1,p_1) \circ (g_2,p_2)) \circ (g_3,p_3)$$

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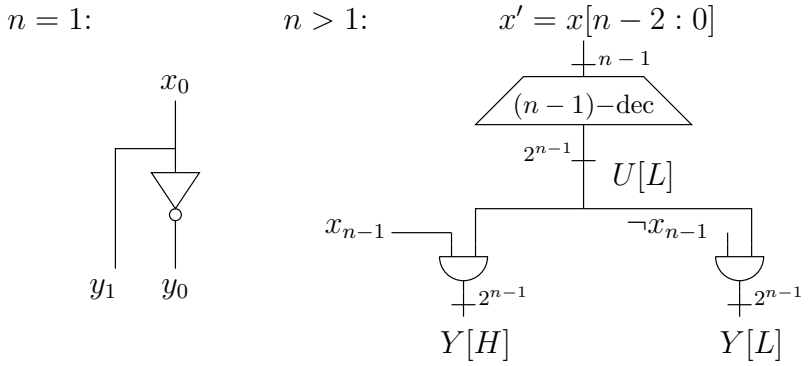
3. Construction a n-CLA with an n-PP$_\circ$. (2 points)

Exercise 2: **(6)**

In the lecture, we constructed an decoder as follows:



which fulfills

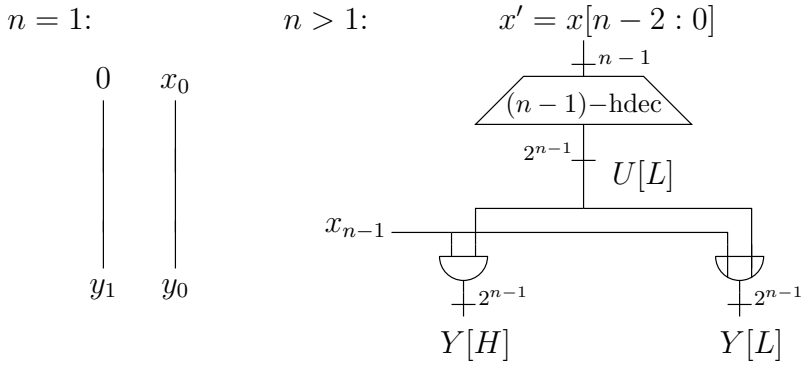
$$y_i = 1 \leftrightarrow \langle x \rangle = i$$

1. Analyse the cost and delay of above construction. (2 points)

2. Construction a faster decoder with logarithmic delay and prove the correctness of your construction. (4 points)

Exercise 3: **(8)**

In the lecture, we also constructed an half decoder as follows:



which fulfills

$$y = 0^{2^n - \langle x \rangle} 1^{\langle x \rangle}$$

1. Analyse the cost and delay of above construction. (2 points)

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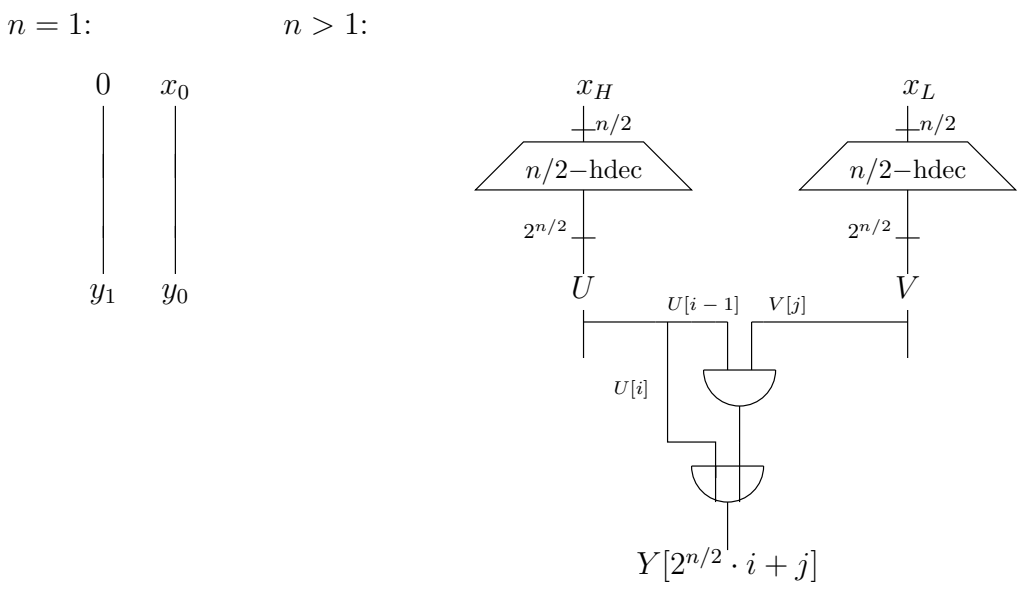
2. The partial construction of a fast half-decoder is presented in the following:



(a) Complete the construction for the case $i = 0$. (2 points)
(b) Prove the correctness of the overall construction of the fast half-decoder. (2 points)
(c) Analyse the cost and delay of the fast half-decoder. (2 points)

Exercise 4: **(4)**

In the lecture, we implemented an cyclic n-left shifter (n-SLC) with a chain of (n, b)-SLCs.

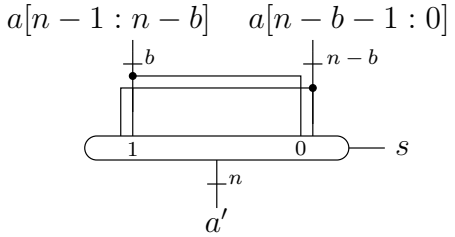


Figure 1: (n, b)-SLC

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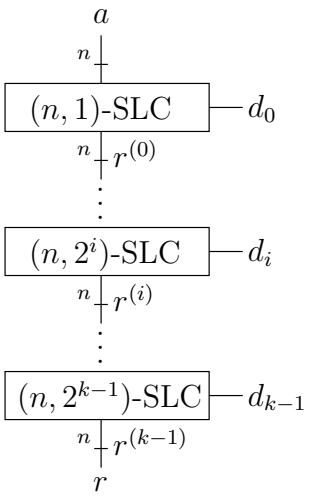

Figure 2: n-SLC

Prove the correctness of n-SLC, i.e.

$$r = a[n - \langle d \rangle - 1 : 0] \circ a[n - 1 : \langle d \rangle]$$