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Department 6.2 - Computer Science
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Multicore System Architecture - WS15/16

Exercise Sheet 12 (due: 5.2.2016)

Tutor: _____

Name, Matr. Number: _____

Exercise 1: **(10)**

Since cache is very expensive, we need to reduce the number of caches in our processor. Currently, we have 4 caches for each core. We want to discard the caches for address translations.

- Consider the case when we share a cache between stage 1 and stage 2, and another cache between stage 5 and stage 6, design the arbiter and control automaton.
- How to design the arbiter and the control automaton if we want to use one cache for each core?