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# Multicore System Architecture - WS15/16

**Exercise Sheet 11 (due: 29.1.2016)**

Tutor: _____

Name, Matr. Number: _____

## Exercise 1: (10)

In the lecture, we redefined the stabilizer circuit.

$$treq_E^{old} = mop.4 \wedge full.4 \wedge mode$$
$$mreq_I^{old} = full_1$$
$$treq_I^{old} = mode \wedge \neg(jisr.6 \wedge full_6)$$

The new stabilizer circuit is defined in Fig.1. We let $Yreq \in \{treq_I, mreq, treq_E\}$. Correspondingly, $Xbusy \in \{mmu_I.busy, mbusy_I, mmu_E.busy\}$.

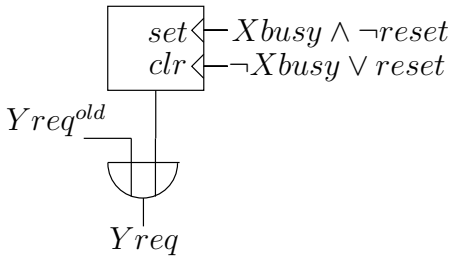


Figure 1: stabilizer circuit

To prove the correctness of our pipeline, we need to prove the following two lemmas:

$$Yreq^t \wedge stall^t \wedge \neg Xbusy^t \wedge \neg freeze^t \rightarrow Yreq^{t+1}$$
$$careq(i)^t \wedge stall^t \wedge \neg Xbusy^t \wedge \neg freeze^t \rightarrow careq(i)^{t+1}$$

$careq(i)$ is the request from cache $i$. These lemmas tell us when access can not discharge, the request should be reactivated. However, this does not work if there is a *rollback*. Explain the reason in words. Then, try to fix the above lemmas and prove them. (6 points) To prove the machine liveness, we need to prove (4 points)

$$I(k,t) = i \rightarrow \exists t' > t.\ I(k+1,t') = i$$

## Exercise 2: (6)

We connect the hard disk interrupt event signal to the external interrupt event signal $e$. We also require as a software condition: if the start disk command is issued in step i and step j is the next disk step, one is only allowed to poll the command and status register of the disk between steps i and j. If we sample $e$ in stage 1.

$$sample(i) = \epsilon\{t \mid I(1,t) = i \wedge ue_1\}$$

Define the external interrupt event signal $e_{isa}$ (2 points). Prove the correctness. (4 points) Note that, in the induction step of the correctness proof, we assume the *reset* signal to be inactive. (Hint: The discovery of $e$ is delayed depending on the number of instructions in the pipe.)