Saarland University
Department 6.2 - Computer Science
Prof. Dr. W. J. Paul
Geng Chen

Multicore System Architecture - WS15/16

Exercise Sheet 1 (due: October 30, 2015)

Important:

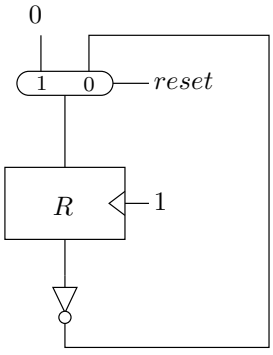
- Each week on Friday one exercise sheet will be released. The solutions should be handed in before or after the next Friday lecture if not stated otherwise. For the admission to the exam you will need at least 50% of the points of the exercises.
- Tutorials: Group A: TBA (Tutor: Jonas Donia) and Group B: Tuesday, 12:00 - 14:00 (E13 328, Tutor: Shahd Zahran)
- You are allowed to solve the exercise sheets in groups. Everybody who has his or her name on the solution must be able to present it in the tutorials. Everybody must present the solution of at least two exercises.
- Please, register for the lecture at the lecture's webpage until Nov 13th, 2015!
  http://www-wjp.cs.uni-saarland.de/lehre/vorlesung/rechnerarchitektur/ws15/anmeldung.php
  Also do not forget to register for the exam in the HISPOS system!
- The oral exam will take place in February. An exact date will be decided upon in class.

Tutor: _____

Name, Matr. Number: _____

Exercise 1: **(2)**

In the following circuit, the *reset* signal is on in cycle $t = -1$ and $\forall t \geq 0.\ reset = 0$.



Prove that the output of the register in cycle t satisfies:

$$\forall t \geq 0.\ R^t = (t\ mod\ 2)$$

Exercise 2: **(4)**

Show that the binary representation $\langle \cdot \rangle : \mathbb{B}^n \to [0 : 2^n - 1]$ is injective. Moreover, prove that it is a bijective mapping.

Exercise 3: **(2)**

A half adder is a circuit satisfying: $\langle c', s \rangle = a + c$. Construct a half adder.

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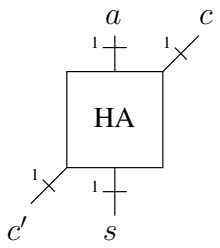


Exercise 4: **(4)**

We let

$$a_H = a[n-1:m] \qquad b_H = b[n-1:m]$$
$$a_L = a[m-1:0] \qquad b_L = b[m-1:0]$$

then show that:

1. $\langle a \rangle = \langle a_H \rangle \cdot 2^m + \langle a_L \rangle$
2. Let

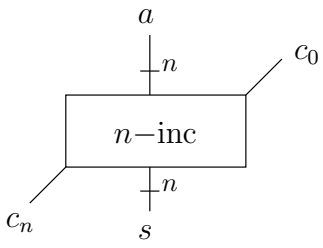
$$\langle c' s_L \rangle = \langle a_L \rangle + \langle b_L \rangle + c_0$$
$$\langle c_n s_H \rangle = \langle a_H \rangle + \langle b_H \rangle + c'$$

then show that:

$$\langle a \rangle + \langle b \rangle + c_0 = \langle c_n s_H s_L \rangle$$

Exercise 5: **(4)**

An n-bit incrementer is a circuit:



satisfying: $\langle c_n, s \rangle = \langle a \rangle + c_0$. Prove that the following recursively defined circuit is an incrementer and estimate the cost and delay. Let $a_H = a[n-1:n/2], a_L = a[n/2-1:0]$.

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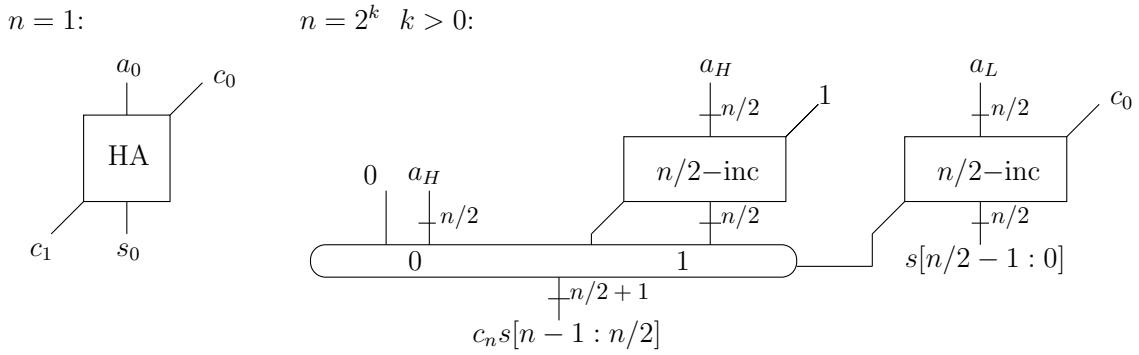


Hint: Use the result of exercise 4.

Exercise 6: **(5)**

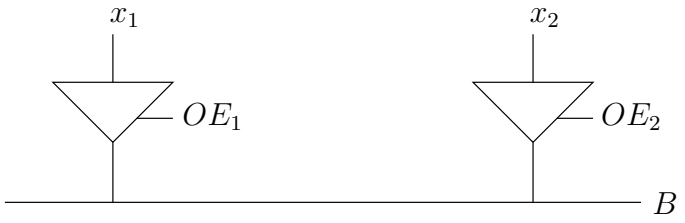
Let $a \in \mathbb{B}^n$. Then, prove the following holds:

$$\begin{aligned}
[0a] &= \langle a \rangle \quad \text{(embedding)} \\
[a] &\equiv \langle a \rangle \bmod 2^n \\
[a] < 0 &\leftrightarrow a_{n-1} = 1 \quad \text{(sign bit)} \\
[a_{n-1}a] &= [a] \quad \text{(sign extension)} \\
-[a] &= [\overline{a}] + 1 \; .
\end{aligned}$$

Exercise 7: **(4)**

Construct hardware for signal OE_1 and OE_2 such that:

$$B^t = \begin{cases} x_1 & t \equiv 0 \; mod \; 4 \\ x_2 & t \equiv 2 \; mod \; 4 \end{cases}$$



Hints: To avoid bus contention,

- at any time t at most one driver produces the signal other than Z;
- don't switch drivers at the same clock edge.

Moreover, a register gives 1 cycle delay.