

Computer Architecture – WS14/15
Exercise Sheet 8 (due: 06.01.15, 40 points)

Exercise 1: (cache quiz) (8 points)

Let ca be a cache of size $k = 8$ (8 entries) and $a = 0^{25}1100$ be a line address. In which entry/entries of ca the data for a can be stored if ca is:

- (a) a direct mapped cache?
- (b) a 2-way associative cache?
- (c) a 4-way associative cache?
- (d) a fully associative cache?

Are there other line addresses that can be stored in the same entry? If yes, give a “formal definition” of the set of such addresses. You are allowed to draw pictures and introduce new notation.

Exercise 2: (fully associative cache) (8 points)

In the lecture we considered the direct mapped and the k -way associative cache types. In this exercise we consider the *fully associative* cache type.

- (a) Give a construction of the fully associative cache capable of storing 2^α lines.
- (b) Show (make sure to have this property!) that the *concrete hit* is unique for design from (a).
- (c) For implementation from (a) derive an abstraction which has a semantics of the *abstract cache*.

Exercise 3: (replacement strategy) (12 points)

In the k -way associative cache the replacement policy is free to choose any of the k entries in the cache to hold the data of a single cache line. Construct a simple k -way associative cache via filling the template from Figure 1.

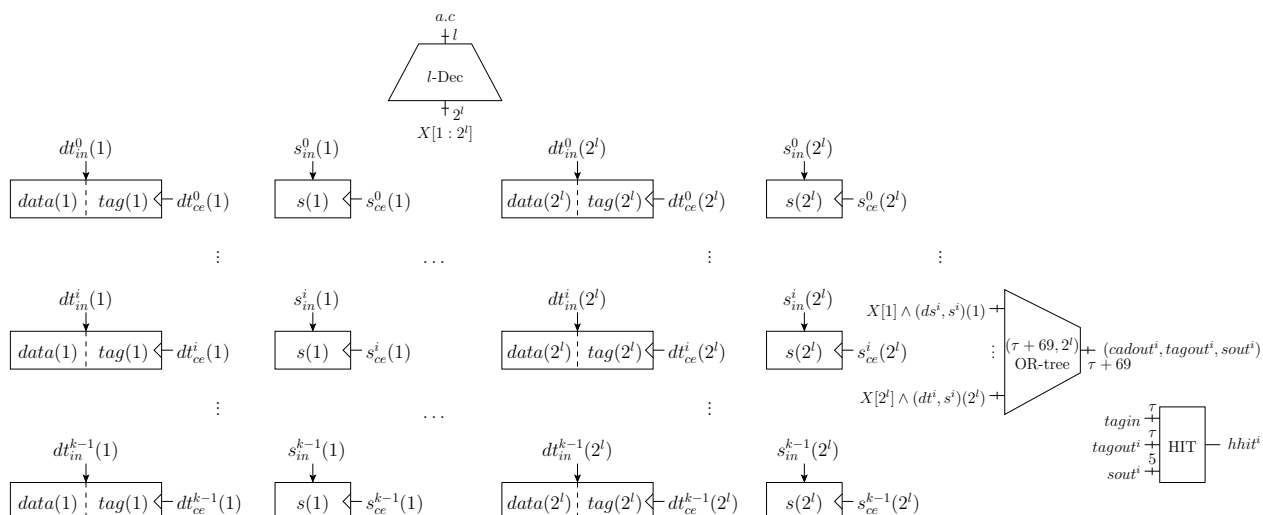


Figure 1: Construction template for the k -way associative cache

- (a) Finish the construction (specify signals). Prove that it implements a k -way associative cache.
- (b) Make sure the construction implements the FIFO replacement strategy. Turn it into the LRU.

Exercise 4: (memory abstraction) (8 points)

Show that the following definition of an implemented memory m is well-defined (or prove that it is not well-defined and discover missing invariants).

$$m(a) = \begin{cases} aca(i).data(a) & ahit(aca(i), a) \\ mm(a) & \text{otherwise} \end{cases}$$

Exercise 5: (memory consistency) (4 points)

Explain (in words) how you understand the *sequential consistency* property of the memory system.