

**Computer Architecture – WS14/15**  
**Exercise Sheet 6 (due: 09.12.14, 24 points)**

---

**Exercise 1: (correctness proof) (10 points)**

Recall in the last exercise you were supposed to prove some proof obligations for the “simple” pipeline (without forwarding and stalling). Now, we add forwarding and stalling engines. Repeat that proof, i.e., for register  $X \in \{A, B\}$  and  $i = I(2, t)$  show the following:

$$X_{in\ \pi}^t = X_{in\ \sigma}^i.$$

In your proof argue about all possible cases where instructions  $I^{i-1}$ ,  $I^{i-2}$  and  $I^{i-3}$  modify the content of the required GPR register. Explicitly point the places where you rely on the correctness of the forwarding / stalling hardware. In the proof you are allowed to use for the “pipeline with bubbles” the following result from the book:

$$\forall k \in [3 : 5] : \quad I(k, t) = I(2, t) - \sum_{j=2}^{k-1} full_j^t.$$

Attention: do not forget to argue about the load from the memory.

**Exercise 2: (timing conditions) (10 points)**

In the lecture we considered a detailed hardware model, where time is real valued and circuit signals (which include register outputs) are functions from time to  $\{0, 1, \Omega\}$ . We introduced the following parameters of the model:

- the position  $\gamma$  of clock edge 0;
- the cycle time  $\tau$ . For  $c \in \mathbb{Z}$  this defines the position  $e(c)$  of clock edge  $c$  as

$$e(c) = \gamma + c \cdot \tau;$$

- $\rho$ : the minimal propagation delay of register outputs after clock edges;
- $\sigma$ : the maximal propagation delay of register outputs after clock edges ( $0 \leq \rho < \sigma$ );
- $ts$ : setup time of register input and clock enable before clock edges;
- $th$ : hold time of register input and clock enable after clock edges;
- $\alpha$ : minimal propagation delay of gates;
- $\beta$ : maximal propagation delay of gates ( $0 < \alpha < \beta$ ).

We have also defined the minimal and the maximal propagation delay of an arbitrary signal  $y$ :

$$\begin{aligned} tmin(y) &= \rho + sp(y) \cdot \alpha \\ tmax(y) &= \sigma + d(y) \cdot \beta \end{aligned}$$

and introduced the timing conditions which must be satisfied in order for the detailed model to behave like a digital (abstract) one:

1.  $\forall y : tmax(y) + ts \leq \tau,$
2.  $\forall i : tmin(x[i]in) \geq th \wedge tmin(x[i]ce) \geq th.$

In this exercise you need to consider the circuit from Figure 1 and do the following (assume  $\tau = 20$ ):

- Choose some (non-zero) values for all parameters of the model, such that the timing conditions for all signals are satisfied (provide calculations for every signal).
- Draw a timing diagram, showing values of all signals for two cycles starting from  $\gamma$ . You may assume  $x[0]^\gamma = a_0 \in \mathbb{B}$  and  $x[1]^\gamma = a_1 \in \mathbb{B}$ .
- Choose some (non-zero) values for all parameters of the model, such that the second timing condition for the signal  $x[0]ce$  is violated. Draw a timing diagram (two cycles starting from  $\gamma$ ), showing what happens with the signal  $x[0]$  in this case.

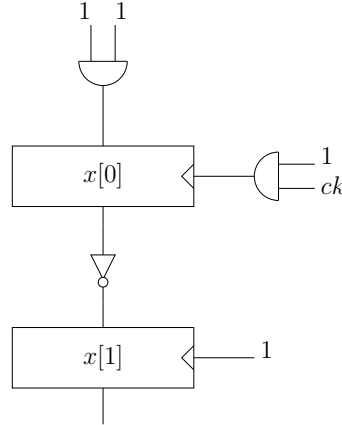


Figure 1: Simple circuit with two registers

**Exercise 3: (regular and hold times) (4 points)**

Assume  $hold(y, t)$  and there are some  $t_1, t_2 \in [t - \alpha, t]$ , s.t.

$$reg(y, t_1) \wedge reg(y, t_2).$$

Show, that under these assumptions for all inputs  $z$  of  $y$  the following property holds:

$$z(t_1) = z(t_2).$$