Saarland University
Department 6.2 – Computer Science
Prof. Dr. W. J. Paul
M. Sc. Petro Lutsyk

Computer Architecture – WS14/15

Exercise Sheet 5 (due: 02.12.14, 24 points)

Exercise 1: (no self-modification) (6 points)

In the lecture we introduced two memory regions:

- $CR \subset \mathbb{B}^{29}$ — code region, and
- $DR \subset \mathbb{B}^{29}$ — data region.

(a) Explain (in words) what intuition was behind this decision.

(b) Give a *software condition* "no self-modification".

(c) Explain (in words) how the software condition above helps to argue in the correctness proof.

Exercise 2: (delay slot) (6 points)

In the lecture we changed the MIPS semantics, s.t. now the instruction is fetched from the *delayed pc*:

$$\begin{aligned} c'.dpc &= c.pc \\ I(c) &= c.m_4(c.dpc) \end{aligned}$$

- Explain (in words) what the *delay slot* is.
- Show that the link address

$$linkad(c) = c.pc +_{32} 4_{32}$$

is still computed correctly in case of jump-and-link instructions

$$jal(c) \vee jalr(c),$$

i.e. we do not fetch the same instruction twice.

Exercise 3: (scheduling functions) (6 points)

Recall definition of the scheduling functions from the lecture:

$$\begin{aligned} \forall k \in [1:5] \quad I(k,0) &= 0 \\ I(1,t+1) &= I(1,t)+1 \\ \forall k \in [2:5] \quad I(k,t+1) &= \begin{cases} I(k-1,t) & ue_k^t \\ I(k,t) & \text{otherwise} \end{cases} \end{aligned}$$

For the "simple" *stall engine*

$$\begin{aligned} \forall t \quad full_0^t &= 1 \\ \forall k \in [1:4] \quad full_k^{t+1} &= \begin{cases} 0 & reset^t \\ full_k^t & \text{otherwise} \end{cases} \end{aligned}$$

prove the following lemmas:

(a)
$$I(k,t+1) = I(k,t) + \begin{cases} 1 & ue_k^t \\ 0 & \text{otherwise} \end{cases}$$

(b)
$$I(k,t) = I(k-1,t) - \begin{cases} 1 & full_{k-1}^t \\ 0 & \text{otherwise} \end{cases}$$

Exercise 4: (correctness proof) (6 points)

In this exercise we derive proof obligations for the instruction memory and register $X \in \{A, B\}$.

For instruction $i = I(k, t)$ show the following:

(a) $$ima^t_\pi = ima^i_\sigma \qquad (k = 1)$$

Hint: split cases on where the instruction in hardware is fetched from (pc or dpc).

(b) $$X^t_{in\,\pi} = X^i_{in\,\sigma} \qquad (k = 2)$$

Stress the place where a software condition is required.