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Computer Architecture – WS14/15
Exercise Sheet 10 (due: 20.01.15, 30 points)

Exercise 1: (physical limitations) (4 points)

Clocking frequency is 2 *GHz*. What is the lower bound for the number of hardware cycles required for the signal to be transmitted over the bus of

(a)   length 10 *cm*?

(b)   length 20 *cm*?

Exercise 2: (computation of protocol signals) (6 points)

In the lecture we have specified circuits $C1$, $C2$, and $C3$ informally. In this exercise you need to provide formal specification (i.e. define the outputs as functions of the inputs) of

(a)   circuit $C1$.

(b)   circuit $C2$.

(c)   circuit $C3$.

Exercise 3: (improvement of implementation) (12 points)

Recall that according to the protocol specification (tables) in case of a miss the required data are obtained either from another cache (by data intervention) or from the main memory. Assume the required data are shared among several caches. Moreover, assume these data do not have an owner. In this case the protocol (implicitly) specifies to retrieve data from the memory, which is a drawback, since accesses to dynamic RAMs are much slower than accesses to caches.

(a)   Argue why exactly this is happening.

(b)   Explain (in words) how you can improve the performance in this case without changing the specification. You are allowed to introduce additional hardware components (just specify them).

(c)   Assume you have complete correctness proof of the original design (one presented in the script). What would be the key argument that you add to prove the correctness of the modified design.

Exercise 4: (properties of protocol) (8 points)

Let acc be a read access ($acc.r$) to port i and $a = acc.a$. Show that

(a)   possible changes to slice a depend only on slice a:

$$\forall ms_1, ms_2 : \Pi(ms_1, a) = \Pi(ms_2, a) \rightarrow \Pi(\delta_1(ms_1, acc, i), a) = \Pi(\delta_1(ms_2, acc, i), a)$$

(b)   answer of the memory system depends only on slice a:

$$\forall ms_1, ms_2 : \Pi(ms_1, a) = \Pi(ms_2, a) \rightarrow pdout1(ms_1, acc, i) = pdout1(ms_2, acc, i)$$