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Computer Architecture I - WS 07/08

Exercise Sheet 7

Excercise 1: (pipelining)

1. Explain the idea of pipelining.
2. Which two main problems do we face converting our sequential DLX implementation into a pipelined one. Solutions?

Excercise 2: (delay slots)

1. What are delay slots?
2. The delay slots should be filled either with NOP (NOOP) instructions (means: "no operation") or with some useful operations. The semantic of a NOP instruction is simple: it should only increase the PC and should not change all other components. What can we use as a NOP instruction without introducing new instructions into ISA? Show at least 10 different examples.
3. Let `nop` be some NOP instruction from the previous exercise and a some memory address. Consider the following assembler program:

```
a+4  :  lw RD=r1,RS1=r0,imm=400
a+8  :  lw RD=r2,RS1=r0,imm=401
a+12 :  addi RD=r3,RS1=R0,imm=0
a+16 :  beqz RS1=r1,imm=24
a+20 :  nop
a+24 :  add RD=r3,RS1=r3,RS2=r2
a+28 :  subi RD=r1,RS1=r1,imm=-1
a+32 :  j imm=-16
a+36 :  nop
a+40 :  sw RD=r3,RS1=r0,imm=403
```

   What does this program compute? Rewrite it without any NOP instruction.