Saarland University
Department 6.2 - Computer Science
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Computer Architecture I - WS 07/08

Exercise Sheet 3

Excercise 1: (warm up)
Prove:

1. $\forall n \in \mathbb{N}^+ : \langle 1^n \rangle = 2^n - 1$.
2. A binary tree of depth m has at most 2^m leaves.
3. In the lecture we have defined the generation and propagation bits in the following way:

$$\begin{aligned} g_{i,i}(a,b) &= a_i \wedge b_i \\ p_{i,i}(a,b) &= a_i \oplus b_i \end{aligned}$$

   Define this bits for $i = 0$.

Excercise 2: (cost and delay computation)

1. Compute the cost and delay of the carry lookahead adder as a closed formula.
2. Recall the carry chain adder construction from the exercise 2.6. Compute the cost and delay of it as a closed formula.
3. An n-bit decoder is a circuit which takes an input $a[n-1:0]$ and computes an output $y[2^n - 1 : 0]$ with the following property:

$$unary(y) \wedge \langle a \rangle = \langle y \rangle_u$$

   (a) Construct an n-bit decoder and prove its correctness.
   (b) Compute the delay and the cost of your construction as a closed formula in n.

Excercise 3: (parallel-prefix computation, carry-lookahead adder)
In the construction of the carry-lookahead adder, we have computed the prefix over the following function $\circ : M \times M \rightarrow M$ for $M = \mathbb{B}^2$ in a parallel prefix circuit:

$$(g1, p1) \circ (g2, p2) = (g2 \vee g1 \wedge p2, p1 \wedge p2)$$

Show that $\circ$ is associative, i.e., $(x \circ (y \circ z)) = ((x \circ y) \circ z)$ for all $x, y, z \in M$.

Excercise 4: (parallel-prefix computation)
Let $u2hu : \mathbb{B}^n \rightarrow \mathbb{B}^n$ be a function that assigns each input bit vector a with $unary(a)$ its half-unary representation. Hence,

$$u2hu(a) = b \text{ such that } unary(a) \wedge \langle a \rangle_u = \langle b \rangle_{hu}$$

1. Construct a simple circuit with cost and delay in $O(n)$ that computes the function $u2hu$. Prove the correctness of your construction.
2. Construct a parallel-prefix circuit that computes $u2hu$ and prove its correctness. Furthermore, compute the delay and the cost of your construction as a closed formula.
3. Draw the PP-circuit for $n = 8$.

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Excercise 5: (optimization of an 4/2-adder)
The 4/2 adder presented in class has a delay of two full adders.

1. Analyse the output paths and try to optimize the delay of your construction.
2. Prove that your construction is still correct.

Appendix

Let $a \in \mathbb{B}^n$ be a bitvector. We define two predicates on it:

$$\begin{aligned} unary(a[n-1:0]) &= (a[n-1:0] = 0^{n-i-1}10^i) \text{ for some } i \in \{0, ..., n-1\} \\ halfunary(a[n-1:0]) &= (a[n-1:0] = 0^{n-i}1^i) \text{ for some } i \in \{0, ..., n\} \end{aligned}$$

That is, $unary(a)$ indicates that exactly one bit of a is set, and $halfunary(a)$ indicates that all bits of a from some position i are ones to the right and zeros to the left. Moreover, we introduce two functions $\langle \cdot \rangle_u$ and $\langle \cdot \rangle_{hu}$ which interpret unary and halfunary bitstrings as natural numbers in the following way:

$$\begin{aligned} unary(a[n-1:0]) &\Rightarrow a[n-1:0] = 0^{n-i-1}10^i &&\Rightarrow \langle a[n-1:0] \rangle_u = i \\ halfunary(a[n-1:0]) &\Rightarrow a[n-1:0] = 0^{n-i}1^i &&\Rightarrow \langle a[n-1:0] \rangle_{hu} = i \end{aligned}$$

Examples:

$$\begin{aligned} \langle 000001 \rangle_u &= 0 \\ \langle 001000 \rangle_u &= 3 \\ \langle 000000 \rangle_{hu} &= 0 \\ \langle 001111 \rangle_{hu} &= 4 \end{aligned}$$