University of the Saarland
Department 6.2 - Informatik
Prof. Dr. W.J. Paul

Computer Architecture I - WS 03/04

(due: 14.01.2004)

Exercise 1: (List of predicates) **(6 points)**

Make a list of all signals (predicates) which are used in the different stages of the DLX sequential machine.
Give signals you need for each stage. Which signals have to be pipelined to the different stages? Mark predicates that you need in more than one stage.

Exercise 2: (Mask circuit) **(10 points)**

- Specify a mask circuit for load operation (see lecture). The circuit should take *lresult* (shifted data from data memory) and necessary control signals and it should return the correct result of load operation *sh4l* to be stored in GPR.
- Specify and analyze a layout for this circuit.

Exercise 3: (Data memory write signals) **(8 points)**

- Specify circuit for computation of data memory write signals $dmw^{(i)}$.
- Specify and analyze a layout for this circuit.

Exercise 4: (assembler programming) **(6 points)**

Let $n, a_1, \ldots, a_n$ and $b_1, \ldots, b_n$ be natural numbers. Write a DLX assembler program which computes the sums $s_i = a_i + b_i$.
At the start of your program n will be stored in register $GPR[1]$, a_i in the memory cell $M(i-1)$ and b_i in the memory cell $M(n+i-1)$, where $i \in \{1, \ldots, n\}$. Your program should store result s_i in the memory cell $M(2n+i-1)$ for all $i \in \{1, \ldots, n\}$.
Find a way to show whether overflow by computing s_i has happened.
Comment your program in a way that everyone can understand what it should do. Programs without a enough comments will give 0 points!!!