

Exercise 1: (alternative layout)

(3+3+2+1 points)

Consider an alternative layout for the multiplication array without using trees for inputs $a[n-1:0]$ and $b[m-1:0]$. Instead of using layout (a), construct the multiplication array as (b) (see Figure 1).

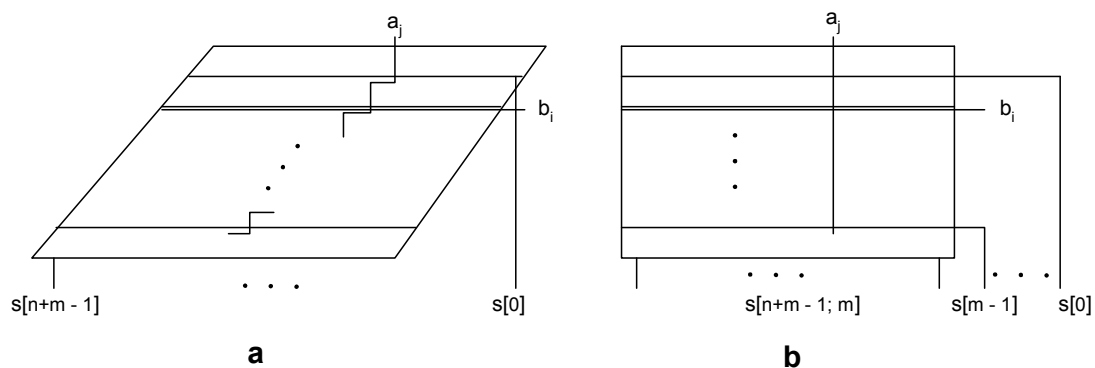


Figure 1: Layouts for the multiplication array

- Specify connections inside the array.
- Compute width of layout (b).
- Compare values of width for both layouts in the case $m = n$.
- Compute values of width for both layouts for cases:
 - $m = n = 32$
 - $m = n = 58$

Exercise 2: (full adder)

(4+4+3+3 points)

In the lecture we presented the VLSI model with some changes, namely we consider only gates as small circuits.

Specify two different layouts for the full adder:

- minimize area for the first one
- minimize delay for the second one
- specify parameters for both cases (width, height, delay, locations of inputs/outputs, loads of inputs)
- estimate the maximal value of δ according to input/output locations for both cases



Computer Architecture I - WS 03/04
 (due: 3.12.2003)

Exercise 3: (carry chain adder)

(3+3+4+2 points)

- Specify a simple layout for carry chain adder (use one row of full adders¹). Compute width, height, area, input loads and delay for this layout.
- Do the same for a layout which uses two rows of full adders.
- Consider parameterized layout depending on s , where s is a number of rows of full adders (see Figure 2). Derive formulas for width $w(n, s)$, height $h(n, s)$, area $area(n, s)$, input loads $L(n, s, i)$ for all inputs i and delay $time(n, s)$.
- Compute these formulas for the following specific values of parameters:

	$n = 32$	$n = 56$
$\delta = \nu = 1/3$		
$\delta = \nu = 1/20$		

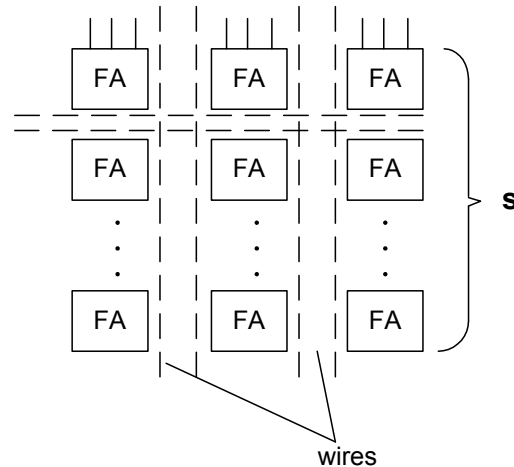


Figure 2:

¹You can use any of your constructions from the Exercise 2