University of the Saarland

Department 6.2 - Informatik

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Computer Architecture I - WS 03/04

(due: 26.11.2003)



Exercise 1: (weight of nodes in the addition tree)

(5 points)

In the lecture we defined the weight $w(\nu)$ of a node ν in the addition tree of multipliers by:

- For leaves: $w(\nu) = \begin{cases} 3 \text{ for } 3/2 \text{ adders} \\ 4 \text{ for } 4/2 \text{ adders} \end{cases}$
- For an inner node ν with left father x and right father y:

$$L(\nu) = w(x)$$

$$R(\nu) = w(y)$$

$$w(\nu) = L(\nu) + R(\nu)$$

Show by induction on the level l in the addition tree, that for two nodes ν and ν' on the same level l, such that the node ν is left of ν' we have:

$$w(\nu) \le w(\nu')$$

Exercise 2: (cheapest full adder)

(4 points)

The full adder we use has cost 14 (see lecture). Can you find a cheaper one? You can use NOT, AND, NAND, OR, NOR, XOR, NXOR, MULTIPLEXOR (MUX) gates in your construction. The costs of these gates is defined in the following table:

gate	NOT	AND, NAND	OR, NOR	XOR, NXOR	MUX
Cost	1	2	2	4	3

Exercise 3: (top-level connection)

(4 points)

In the lecture we considered the construction of an addition array in a simple VLSI hardware model¹. The layout was based on two kinds of boxes: a box for an inner full and a box on the top of array. Also we specified connections between them inside of the array. Specify connections on the top of the array and give the height of a whole column of the matrix.

Exercise 4: (CLA in VLSI model)

(3+5+4 points)

Realize an n-bit Carry Look Ahead adder in the VLSI model:

- by specifying boxes needed the constructing (geometries, inputs/outputs location, cost)
- and specifying an arrangement and connections of these boxes to build carry look ahead adder
- compute cost and delay for your construction

Note:

- 1. cost of a small circuit SC(S) < 20
- 2. relation height/width $1/2 \le \frac{h(S)}{b(S)} \le 2$

¹see also On the complexity of Booth Recoding in our internet page under Bibliography