

Exercise 1: (cost of parallel prefix computation)

(3 + 4 points)

Derive a closed formula (without recursion or \sum symbols) for the cost of the parallel prefix circuit from figure 1. For simplicity you can assume that $n = 2^l$ is a power of two. Proof the correctness of your formula by induction on l .

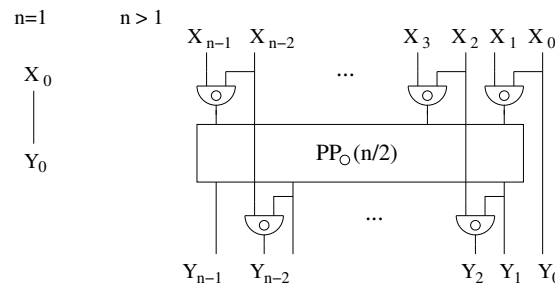


Figure 1: Parallel Prefix Circuit

Exercise 2: (basic properties of two's complement numbers)

(6 points)

In the class two's complement numbers and their properties were presented and one of the properties was proved.

In this exercise you need to prove the others:

$$\begin{aligned} [0a] &= \langle a \rangle \\ [a] &\equiv \langle a[n-2:0] \rangle \text{mod } 2^{n-1} \\ [a] &= \langle a \rangle \text{mod } 2^n \\ [a_{n-1}a] &= [a] \end{aligned}$$

Exercise 3: (compound adder)

(3 + 4 + 3 points)

In figure 2 you see the recursive construction of a compound adder (*add2*) with inputs $a[n-1:0]$ and $b[n-1:0]$, where $m = \lceil n/2 \rceil$ and $k = \lfloor n/2 \rfloor$. This circuit computes simultaneously $\langle s^0 \rangle = \langle a \rangle + \langle b \rangle$ and $\langle s^1 \rangle = \langle a \rangle + \langle b \rangle + 1$. The 1-bit compound adder is constructed using OR, XNOR (negated XOR) gates to compute S^1 and AND, XOR gates to compute S^0 .

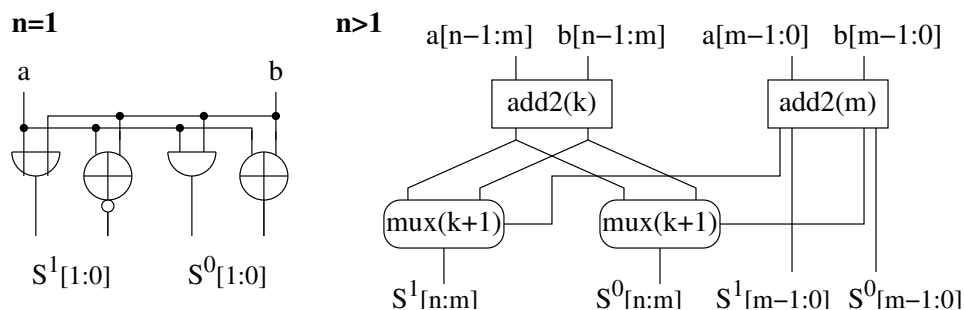


Figure 2: Compound Adder

1. Compute cost and delay of a n bit compound adder in a closed formula (without recursion and \sum symbols). You can assume that n is a power of two and cost and delay of the basic gates (AND, OR, XOR, XNOR) are 1. Cost of a n -bit multiplexer is $3n$. Its delay is 2.



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2. Prove the correctness of your formulas by induction.
3. Give a recursive construction (draw a circuit) of a n -bit conditional sum adder (on the base of the compound adder) that computes the sum for inputs $a[n-1:0]$, $b[n-1:0]$ and carry c_{in} .

The conditional sum adder behaves in the following way:

Let $m = \lceil n/2 \rceil$ and $k = \lfloor n/2 \rfloor$ and

$$s[n:0] = s[n-1:m]s[m-1:0]$$

then

$$\langle s[n:m] \rangle = \langle a[n-1:m] \rangle + \langle b[n-1:m] \rangle + c_{m-1}$$

$$= \begin{cases} \langle a[n-1:m] \rangle + \langle b[n-1:m] \rangle & \text{if } c_{m-1} = 0 \\ \langle a[n-1:m] \rangle + \langle b[n-1:m] \rangle + 1 & \text{if } c_{m-1} = 1 \end{cases}$$

Excercise 4: (zero tester)

(3 + 4 points)

We need to construct a circuit which takes n -bit string as argument and returns 1 if all input bits are zeros and 0 otherwise. Give the circuit, its cost and delay for arbitrary n (try to achieve minimal delay). Prove correctness of your formulas.