University of the Saarland
Department 6.2 - Informatik
Prof. Dr. W.J. Paul

Computer Architecture I - WS 03/04

(due: 11.02.2004)

This is the last exercise and it should be handed out in TWO weeks.

In the internet site there is a high level circuit of the current sequential DLX.

Exercise 1: (Instruction Decoder Layout) **(9 points)**

Specify and analyze a layout for Instruction decoder. Your ID should provide the following signals:

rtype	– an instruction of R-type
jtype	– an instruction of J-type
link	– a link instruction (*jal* or *jalr*) (used in *bjtaken* computation, as select signal between data from the link register and ALU-Shifter block)
shi	– a shift instruction using shift amount SA (used in constant computation)
jreg	– a jump register instruction (*jr* or *jalr*) (used in next PC computation)
sh	– any shift instruction (used to get result either from ALU or from Shifter)
rop	– any arithmetic or logic operation using immediate constant or shift using SA (*i-type* or *shi*) (used in order to select right operand for ALU and Shifter)
test	– any test operation (used in ALU)
store	– a store instruction (used in $dmw^{(i)}$-signal computation)
load	– a load instruction (used to select loaded information for storing in GPR)
j	– a jump instruction (used in *bjtaken* computation)
jl	– a jump and link instruction (used in *bjtaken* computation)
beqz	– a branch-equal-zero instruction (used in *bjtaken* computation)
bnez	– a branch-not-equal-zero instruction (used in *bjtaken* computation)
$GPRw$	– the write signal for GPR
$d = 1$	– byte access to the data memory (used in $dmw^{(i)}$-signal computation)
$d = 2$	– half-word access to the data memory (used in $dmw^{(i)}$-signal computation computation)
$d = 4$	– word access to the data memory (used in $dmw^{(i)}$-signal computation)
u	– unsigned load (used in $dmw^{(i)}$-signal computation)
$cop[2:0]$	– operation coding for ALU
$shop[1:0]$	– operation coding for shifter

Exercise 2: (*bjtaken* computation) **(7 points)**

Specify and analyze a layout for the *bjtaken* signal computation. As input parameters you should provide necessary signals from the Instruction Decoder and A' operand. Layout for the zero tester is in the internet page in *Comparator*.

Exercise 3: (ue_i computation for sequential DLX) **(6 points)**

Specify and analyze a layout for computation of ue_i signals ($0 \leq i \leq 4$) for the sequential DLX (use circuit you construct for the last exercise).

Exercise 4: (Shift unit) **(8 points)**

Specify and analyze a layout for the Shift Unit (use circuit you construct for the last exercise).

Don't worry if you don't have your own solutions from the last week, this assignment is for TWO weeks.

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Bonus exercise: (Processor without pipelining) **(25 points)**

In this exercise you need to specify a layout for the whole processor and compute its actual size ($h(P\sigma)$ and $w(P\sigma)$), i.e. your last result shouldn't contain δ, ν , $w()$ or $h()$ -parameter of any circuit: only numerical result.

The whole processor circuit and all necessary blocks are in the internet site except ones from previous exercises - use your own.
For the layouts for *ALU* and *nextPC* only sizes and side of input location are available (it is enough for this exercise). To realize GPR use 3-port RAM, which is also available in the site.

Attention: The circuit of the processor doesn't contain the block for *ue*-signals computation, so you need to build in this block and provide corresponding update signals for all registers.

Note: $\delta = \nu = 1/3$