Universität des Saarlandes
FR 6.2 - Informatik
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Exercise Sheet 8
Computer Architecture II
(Due: Jan 10th, 2012)

Exercise 1: (Circuit Lemma) **(8+2 Points)**

In the lecture it was shown how to abstract from a detailed continous-time hardware model to a discrete-time digital one. There we used among others the following lemma describing the values of signals $g \in Sig$ in a circuit of maximal depth $d = \max d(g)$ in an arbitrary cycle c. For all inputs $x \in In$ we have either $x = 0$ or $x = 1$ or $x = R$, where R is the output of a Register R. If for all such registers, their inputs are stable around clock edge c, i.e.

$$rstable(R_{in}, c) \qquad rstable(R_{ce}, c)$$

then there exists a value $a \in \mathbb{B}$, such that:

$$\forall t \in [e(c) + t_{max}(g), e(c+1) + t_{rpmin}]. \quad g(t) = a$$

a) Prove the lemma by induction on d!

b) What is the constraint on the cycle time τ for the lemma to be applicable?

Exercise 2: (Stability Lemma) **(6+2 Points)**

Now we consider a system consisting of registers which are connected by circuits with maximal depth $d = \max d(g)$. If the cycle time τ and register propagation delay t_{rpmin} are big enough, i.e.

$$\tau \geq t_{rpmax} + d \cdot t_{gpmax} + t_s \qquad t_{rpmin} \geq t_h$$

and for all registers R their input signals $x \in \{R_{ce}, R_{in}\}$ are stable initially, i.e. $rstable(x, 0)$, then they are also stable at all following clock edges:

$$\forall c.\ rstable(x, c)$$

a) Prove the statement above!

b) Why is it justified to assume $rstable(x, 0)$? How is this assumption discharged in the implementation of clocked circuits?

Exercise 3: (Affected Cycle) **(2+3 Points)**

In the definition of the first affected cycle $cy(i)$ on the receiver side for sender edge i, we assumed $t_{rpmax} = 0$ in order to have cleaner definitions.

a) Give two definitions $cy_{min}(i)$ and $cy_{max}(i)$ taking into account the minimal and maximal register propagation delay, respectively!

b) Can it happen that (1) $cy(i) \neq cy_{min}(i)$ (2) $cy(i) \neq cy_{max}(i)$ (3) $cy_{min}(i) \neq cy_{max}(i)$? Explain your answers!

Exercise 4: (Correct Sampling from the Bus) **(4+3 Points)**

We introduced a lemma guaranteeing that if the bit to be sent S^i is kept on the bus by the sender for 8 consecutive cycles without spikes, i.e.

$$\forall t \in [e_s(i) + t_{rpmax}, e_s(i+8)]. \quad B(t) = S^i$$

then it is sampled correctly at seven consecutive cycles by the receiver:

$$\forall k \in [0:6]. \quad R^{cy(i)+k+\beta} = S^i$$

Here β distinguishes two cases:

$$\beta = \begin{cases} 0 & : \quad e_r(cy(i)) \geq e_s(i) + t_{rpmax} + t_s \\ 1 & : \quad \text{otherwise} \end{cases}$$

It was already proven that the signal is on the bus long enough so that the seventh sampling is correct.

a) Prove that the signal is on the bus early enough, i.e.:

$$R^{cy(i)+\beta} = S^i$$

b) Is it possible to sample the S^i correct 8 times in a row? Explain your answer!