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Computer Architecture I – WS 06/07

Exercise Sheet 11 **(due: 29.01.07)**

Exercise 1: (Self-modifying code) **(10 points)**

In class, you have seen the software convention that between an instruction that writes to some address a and an instruction that reads from a there has to be an instruction that empties the pipeline. Formally:

$$\forall i, j\ \forall a.\ i < j \wedge (I_i \text{ writes to } m(a)) \wedge (I_j \text{ fetched from } m(a))$$

$$\Rightarrow \exists k.\ i < k < j \wedge (I_k \text{ empties the pipe})$$

where a is an address in the code region.

In this exercise, you have to implement a mechanism that makes an *rfe* instruction such a draining instruction.

Exercise 2: (Self-modifying code) **(10 points)**

Assume that the software convention from exercise 1 does not hold. Then, one has to speculate that the convention is fulfilled. Hence, in case it is not fulfilled, we have to rollback the computation and draining the pipe.

Implement a circuit that checks for misspeculation, performs a rollback in case of a misspeculation, and drains the pipe.

Exercise 3: (Caches) **(4+4=8points)**

In class, you have seen the following invariant for a direct-mapped write-through cache:

$$\$(line).v \Rightarrow \Big(\$(line).data = mm_\Lambda(\$(line).top, line, 0^\lambda)\Big)$$

Moreover, you have seen the specifications of a sectored cache and a k-way set associative caches.

1. Specify the invariant for a sectored direct-mapped cache.
2. Specify the invariant for a sectored k-way set associative cache

Exercise 4: (RAM construction) **(7 points)**

Construct an single port RAM R with inputs $ad \in \mathbb{B}^a$, $din \in \mathbb{B}^n$, $w \in \mathbb{B}$, and $clear \in \mathbb{B}$. The only output is $dout \in \mathbb{B}^n$. The RAM should be a standard RAM except for the fact that the clear input clears every address, i. e. in case $clear^t = 1$ we have that $R^{t+1}(ad) = 0^n$ for all $ad \in \mathbb{B}^a$.