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Computer Architecture I – WS 06/07

Exercise Sheet 10 **(due: 22.01.07)**

Exercise 1: (interrupt level computation) **(5+5+5 = 15 points)**

In class you have seen the definition of the interrupt level $il(c, eev)$ as

$$il(c, eev) = min\{j | mca(c, eev)[j] = 1\}$$

with $j \in \{0, \ldots, 31\}$.

In this exercise you have to construct a circuit that computes this interrupt level. Hence,

1. Construct a circuit with $mca[31:0]$ as input and output $il[5:0]$ such that
$$\langle il[5:0] \rangle = il(c, eev)$$
2. Compute the delay and cost of your construction as a closed formula.
3. Prove the correctness of your construction rigorously.

Exercise 2: (liveness of the pipelined machine) **(10+10=20 points)**

In this exercise we will start the argumentation about the liveness of the pipelined machine.

Therefore, we will need some definitions. Let $pred$, $pred_u$ be time predicates and t be a cycle.

- $pred$ is called *finite false* iff for all t there exists a $t' \geq t$ such that $pred(t')$ holds. Hence, if $pred(t)$ does not hold, there is a finite $t' \geq t$ such that $pred(t')$ holds. Analogous, a predicate $pred$ ic called *finite true* iff $\neg pred$ is finite false.
- $pred$ is said to *stay until* $pred_u$ from cycle t iff the following holds: Given cycle $t' \geq t$ such that $pred_u$ does not hold for t'' with $t \leq t'' < t'$, the predicate $pred$ holds for t''

$$stays\_unitl(pred, T, pred_u) :\Longleftrightarrow$$
$$\forall t'.t' \geq t : \big(\forall t''.t \leq t'' < t' : \neg pred_u(t'')\big)$$
$$\Rightarrow \big(\forall t''.t \leq t'' < t' : pred(t'')\big)$$

- The time predicate $below\_empty_k(t)$ hold iff all stages below stage k are empty during cycle t

$$below\_empty_k(t) := \forall j.k < j < n : \neg full_j^t$$

In order to argue about the liveness of the machine, we have to show that the *stall* signal of a stage k is finite true. In the following, you have to proof two lemmas which will be needed in a liveness proof of the pipelined machine. The first lemma states that if one stalls a stage long enough, eventually all stages below become empty. The second lemma concludes then that if all stages below some stage k are empty, this stays so until the stage is updated.

1. Let k be a stage number, $k \in \{0, \ldots, n-1\}$. Let the stall signals of all stages below stage k be finite true and let t be a cycle. This implies that there is a cycle $t' \geq t$ such that if the update enable signal is off from t to $t'-1$, the full bits of the stages below stage k are off during cycle t'.

$$\exists t'.t' \geq t : (\forall t'' | t \leq t'' < t' : \neg ue_k^{t''}) \Rightarrow below\_empty_k(t')$$

2. Let k be a stage but not the last. If all stages below stage k are empty during cycle t, this stays so until the output registers of stage k are updated.

$$below\_empty_k(t) \Rightarrow stays\_until(below\_empty_k, T, ue_k)$$