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Computer Architecture I – WS 06/07

Cache Accesses

Figure 1 depicts the case of a 'read-hit'.

Figure 2 depicts the timing diagram for the case of a 'read-clean-miss'. In this case, we do not have to perform a write back and load data directly to the cache. During cycles $T1, \ldots, T6$ the load (line fill) is performed. Data for two segments are loaded in this example. Afterwards, the read operation analogous to the 'read-hit' case is performed.

Figure 3 presents the 'dirty-miss-write' case. There, data has to be written back from the cache to the memory and evicted from the cache (cycles $T1, \ldots, T5$). The eviction address is given on the bus ev. After the eviction, *fill line* analogous to Figure 2 is performed and at last the new data is written.

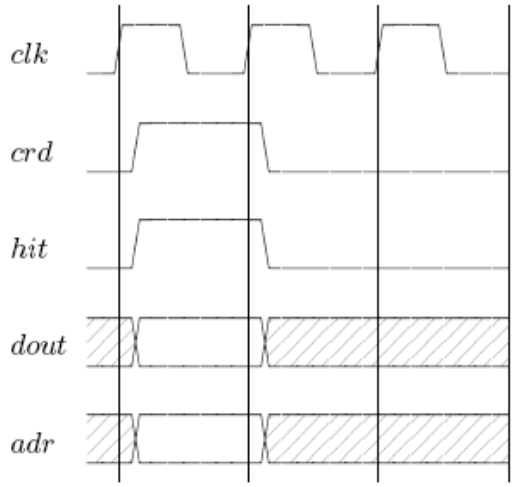

Figure 1: Figure 1: read hit

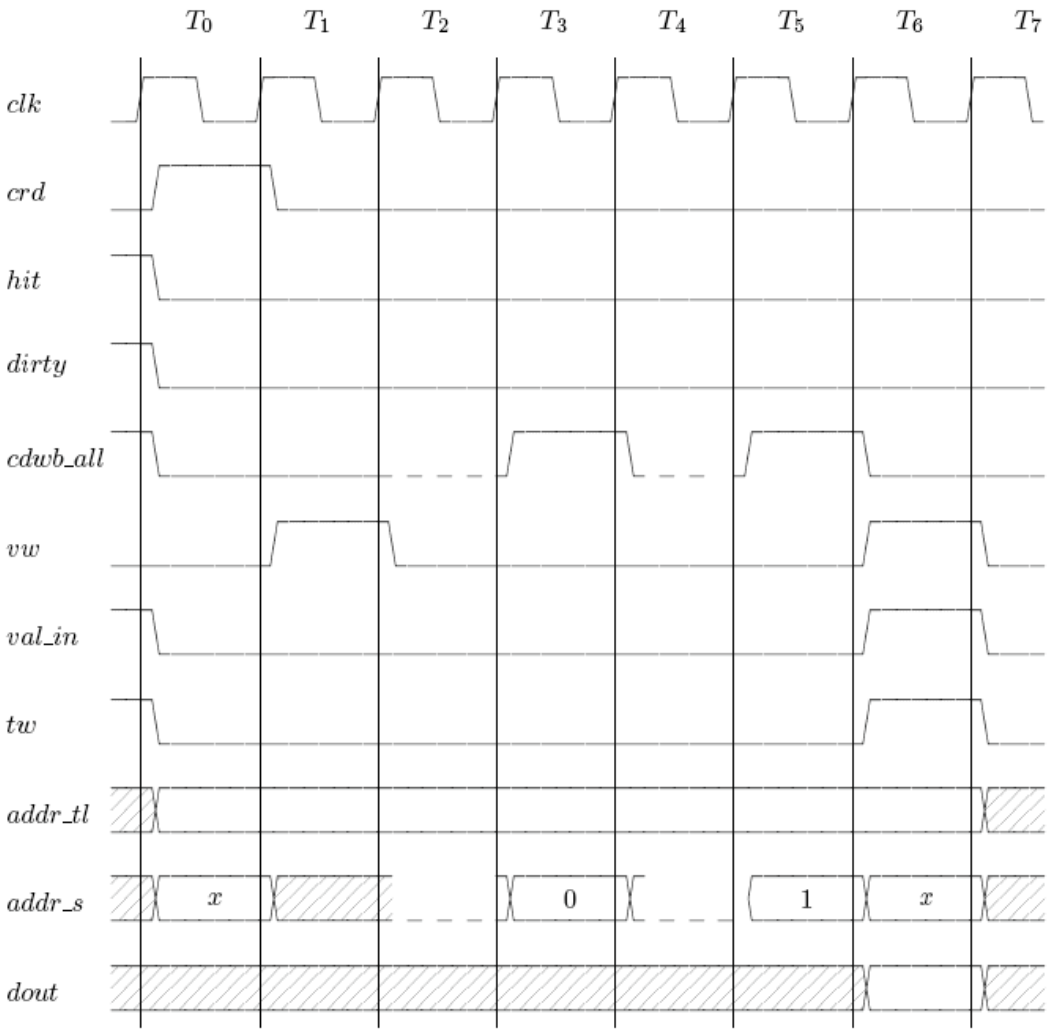

Figure 2: Figure 2: read clean miss

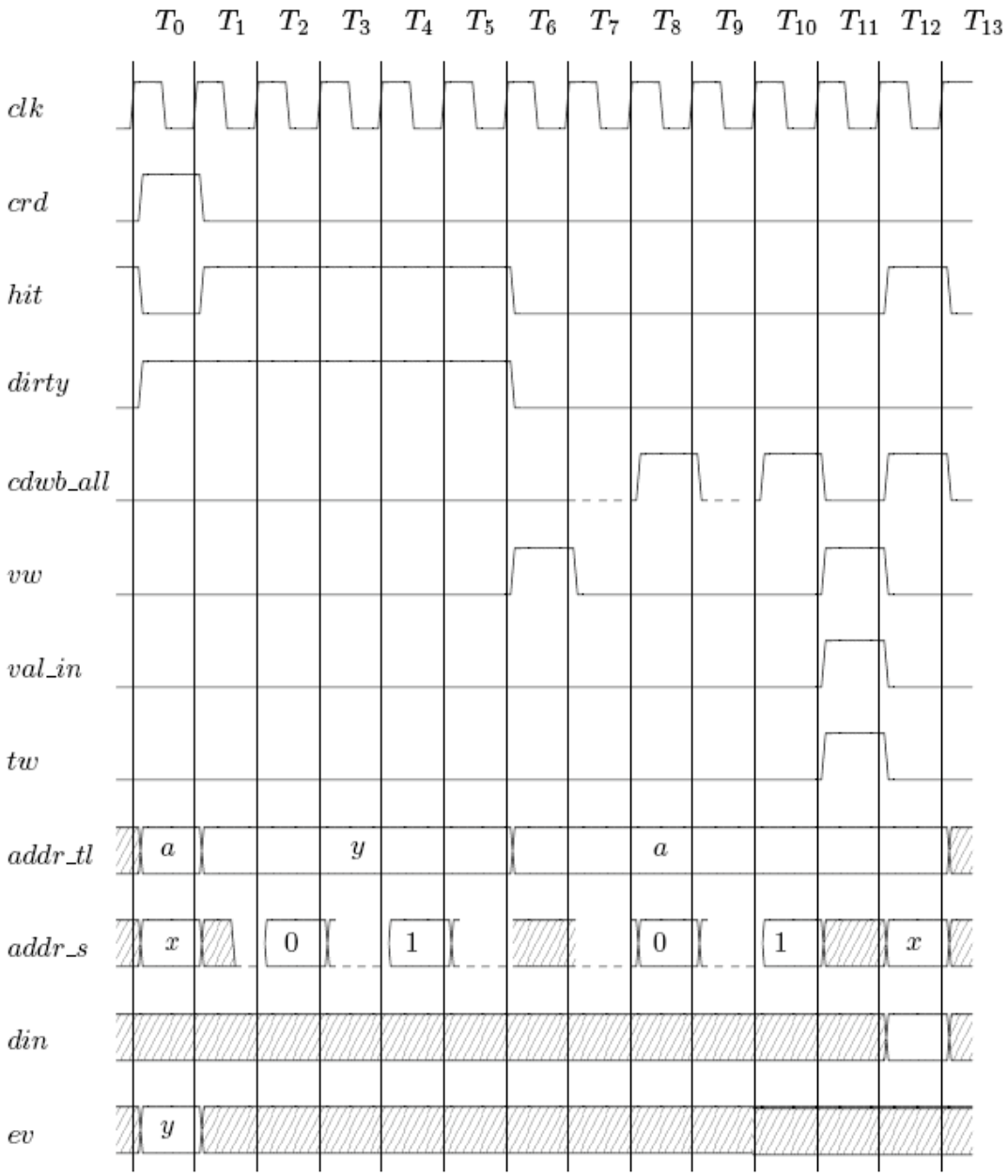

Figure 3: Figure 3: write dirty miss