University of the Saarland
Department 6.2 - Informatik
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Computer Architecture I - WS 02/03

(due: first computer architecture lecture in 2003)

Remember that there are no assignments on december 19th and 20th.

Excercise 1: (Memory Address Register) **(4 points)**

In the proof of the correctness of write accesses to the memory we used the fact that $\mathrm{MAR}^{T+3} = x(k_i)$. Proof the correctness of this formula.

Excercise 2: (List of Predicates) **(6 points)**

Make a list of all control signals of the DLX which are used in the different stages. In which stages are the signals needed? Which bits of the instruction register have to be pipelined to the different stages?
In order to save time/cost some control signals can be precomputed in the instruction decode stages (for example signals which are needed in more than one stage). Mark these signals in your list. Where are they used?

Excercise 3: (Correctness of loads) **(10 points)**

In the lecture we proved the correctness of the execution of store instructions. Do the same proof for load instructions: proof that a load instruction writes the correct data from the memory into the destination register.

Figure 1: Merry Christmas and Happy New Year