University of the Saarland
Department 6.2 - Informatik
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Computer Architecture I - WS 02/03

(due: 09.12.2002)

Excercise 1: (Incrementer) **(2 + 2 + 3 points)**

An incrementer is a circuit which computes from inputs $x \in \{0,1\}^n, c \in \{0,1\}$ the output $y \in \{0,1\}^{n+1}$ with $\langle y \rangle = \langle x \rangle + \langle c \rangle$.

1. Construct an incrementer which is build like a carry chain adder.
2. Give closed formulas for cost and delay of your construction. Proof the correctness of your formulas.
3. Construct an incrementer which is build lika a conditional sum adder. Compute cost and delay of your construction.

Excercise 2: (Program Counter) **(1 + 2 + 2 points)**

A n bit counter is a circuit with inputs *clk* and *reset* and output $y \in \{0,1\}^n$. The output y of cycle $t+1$ is computed by:

If $reset = 0$ then $\langle y^{t+1} \rangle = \langle y^t \rangle + 1 \mod 2^n$ else $y^{t+1} = 0^n$.[1]

1. Construct a n bit counter using an n bit incrementer and a n bit register. Your register has a reset input: when the reset input is 1 the output of the register is set to 0^n.
2. Construct a program counter for the dlx. Depending on the select signal s your counter should be increased by four ($s = 0$) or set to zero ($s = 1$). Use an incrementer circuit for the construction of your counter.
3. Proof that your construction (using an incrementer) correctly adds four to the program counter if s equals 1.

Excercise 3: (Software Multiplication) **(7 points)**

The DLX processor has no fix point multiplier in its arithmetic unit. So there is no instruction for multiplication. Write an assembler program which multiplies the numbers stored in GPR(1) and GPR(2). Your program should store the result in GPR(3).

Excercise 4: (Addresses) **(2 points)**

Because all computations in the DLX are modulo 2^{32} it doesn't matter if the memory chips interpret the addresses generate from the processor as binary numbers or two's complement numbers. The reason for this is that the following equation holds for 32 bit addresses a:

$$[a] \equiv \langle a \rangle \mod 2^{32}$$

Proof the correctness of this formula.

[1] y^t is the value of the output y of the counter after t many clock cycles

Excercise 4: (Von Neumann Adder) **(4 + 3 + 2 points)**

In figure 1 you see the construction of a so called Von Neumann Adder. Its constructed with the two registers Y and X and with $n+1$ many half adders. For a natural number t we denote by X^t and Y^t the value of the registers X AND Y after clock cycle t. So X^0 and Y^0 are the initial values.

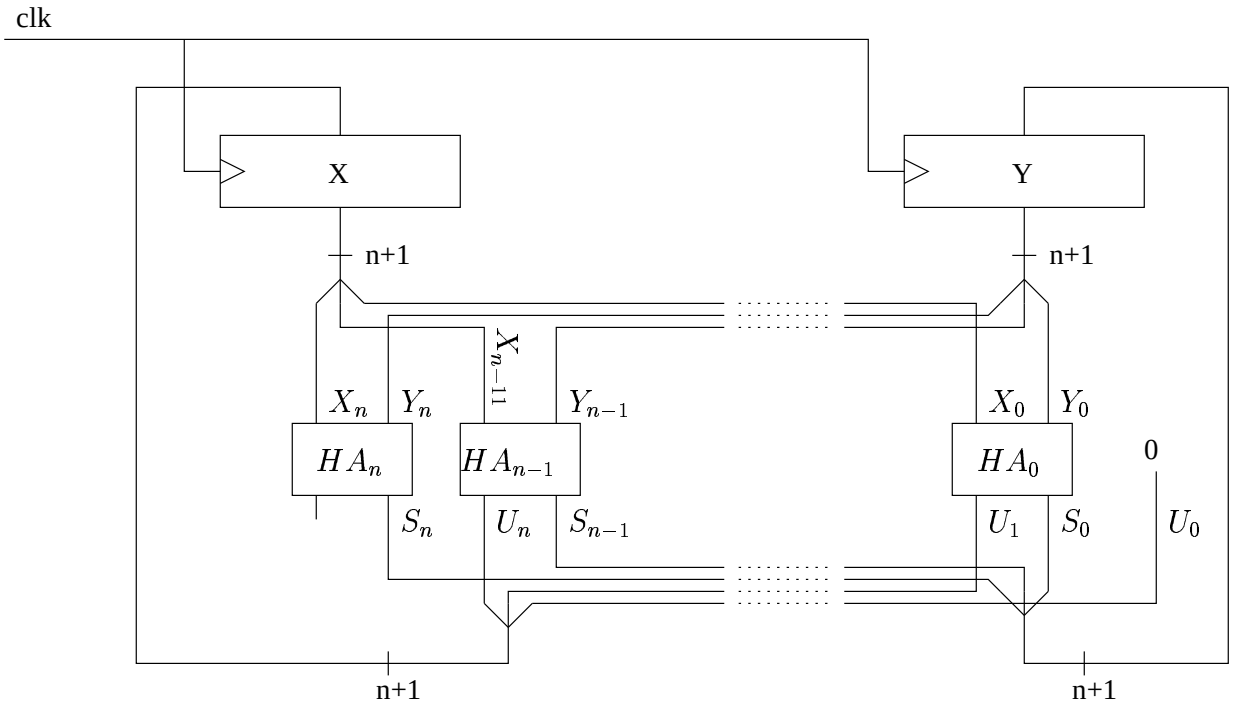

Figure 1: Von Neumann Adder

1. Let the upper most bit be initialized by zero : $X_0^n = 0$ and $y_0^n = 0$. Show the following lemma:
   $\langle X^t \rangle + \langle Y^t \rangle = \langle X^0 \rangle + \langle Y^0 \rangle$ for all $t \geq 0$.

2. Show: $\exists t \leq n+1 : \langle Y^t \rangle = \langle X^0 \rangle + \langle Y^0 \rangle$. This show that the Von Neumann adder needs at most $n+1$ clock cycles to compute the sum of X^0 and Y^0 and to store the result in register Y.

3. In which case does this adder needs exactly $n+1$ cycles for the computation?