



Computer Architecture I - WS 02/03  
 (due: 18.11.2002)

**Excercise 1: (Weights of nodes)**

(8 points)

In the lecture we defined the weight  $W(\nu)$  of a node  $\nu$  in the addition tree of multipliers by:

- For leaves:  $W(\nu) = \begin{cases} 3 & \text{for } 3/2 \text{ adders} \\ 4 & \text{for } 4/2 \text{ adders} \end{cases}$
- For inner nodes with left son  $\lambda$  and right son  $\rho$  :  $W(\nu) = W(\lambda) + W(\rho)$ .

Show by induction on the level  $l$  in the addition tree:

1. In level  $l$  weights are nondecreasing from left to right.
2. The sum of weights of all nodes in level  $l$  is  $m$ .

**Exercise 2: (Leading Zero Counter)**

(8+4 points)

A leading zero counter is a circuit which computes the number of leading zero of a given bit string  $a[n-1:0]$ .

In figure 1 you see two circuits which are helpful for computing the number of leading zeros of  $a$ . In figure 2 you see as an example a leading zero counter for 8 bit inputs that is composed by those two circuits. In a first step the input bits are feed into  $n/2$  many LZero-a circuits and then there is a tree of LZero-b circuits which computes the result  $b[4:0]$ .

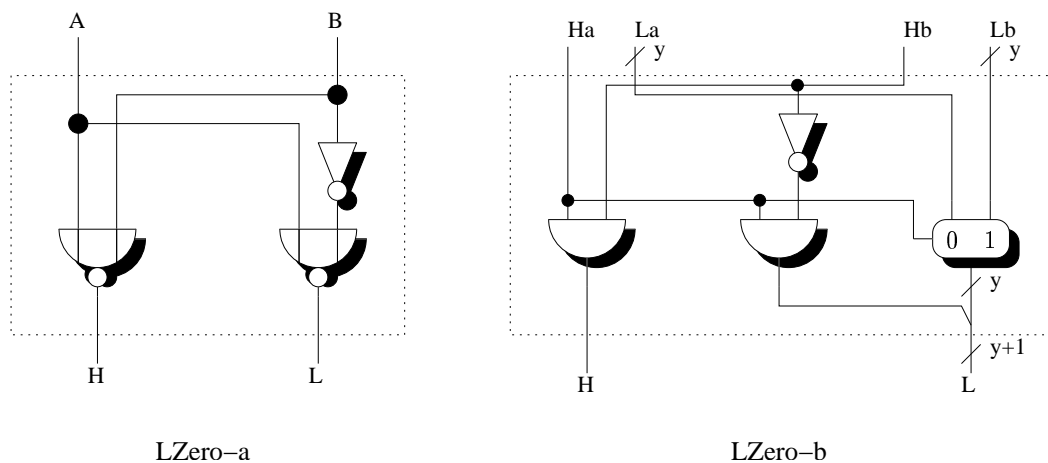


Figure 1: Components for leading zero counter

1. Show that circuits composed in this way compute correctly the number of leading zeros of their input (let  $n$  be a power of two).

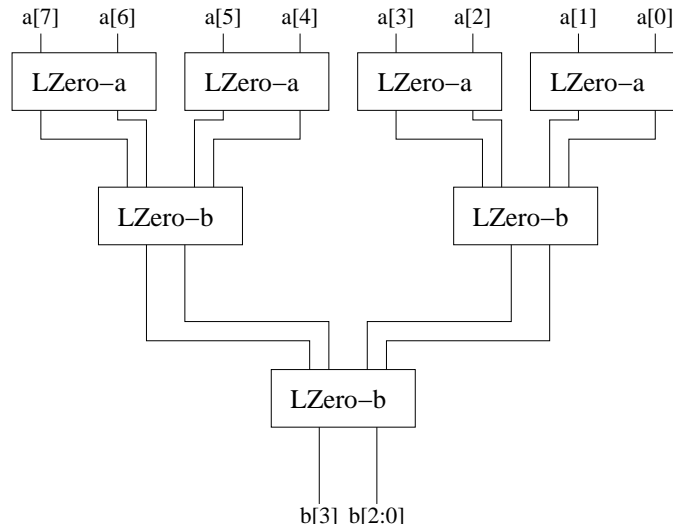


Figure 2: 8 bit leading zero counter

2. Derive a closed formula for the cost and delay of such a circuit. Take as cost for a multiplexer of width  $n$   $C(mux) = 3 * n + 1$  and as its delay  $D(mux) = 3$ . Prove the correctness of your formulae.

**Exercise 3: (Adder Tree)**

**(5+3+2 points)**

In the lecture we build the balanced addition tree of  $n, m$  multipliers with  $4/2$  adders (except the first level where we used  $3/2$  adders and  $4/2$  adders). One can build the addition tree directly with  $3/2$  adders.

1. A  $m/2$  adder adds  $m$  input busses and outputs two output busses. Give a recursive construction of a  $m/2$  adder consisting of  $3/2$  adders. Don't care about the bitwidth of the adders.
2. Derive a formula for the delay of your circuit.
3. For which  $m$  is your delay smaller than the delay of the tree from the lecture?