University of the Saarland
Department 6.2 - Informatik
Prof. Dr. W.J. Paul

Computer Architecture I - WS 02/03

(due: Monday 03.02.2003)

Excercise 1: (Cost and runtime analysis) **(20 points)**

On the lecture website
http://www-wjp.cs.uni-sb.de/lehre/vorlesung/rechnerarchitektur/ws0203/uebungen.php
you can download the cost and runtime programs for the DLX processor (cfiles.tar.gz). Download these programs and make yourself familiar with them.

1. Use the programs to find the critical paths in the following DLX variants:
   - pipelined DLX fixed point core without forwarding (pdlx.c, DLXp=0)
   - pipelined DLX fixed point core with forwarding (pdlx.c, DLXp=1)
   - pipelined DLX fixed point core with forwarding (pdlx.c, DLXp=2)
2. Build a table with the total cost and cycle time of the three variants. What variant is better?
3. Modify the program in a way that cost and cycle time of ALU and shifter environment are output seperately. Make an overview table for these values for the three variants.
4. For the shift4store circuit we used that the lower two bits of the address computation have smaller delay than the other bits in order to minimize the cycle time. Change the program in a way that it outputs the result with and without this trick for all three variants of the DLX and compare the results.