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Computer Architecture I - SS09

Exercise Sheet 9 (due: 13.07.09)

Exercise 1: (bus protocol) (2 points)

In the lecture we considered a synchronous bus protocol used in cache-memory system (see Chapter 6 in the book S. Müller, W. Paul, Computer Architecture, Complexity and Correctness). Assume that we support devices providing the result already in the next cycle after the request so that the hand shake in not needed (in contrast to the fast read/write when $Brdy$ is used). In this exercise you are supposed to provide the timing diagrams of single-word read and write transfer for this case.

Exercise 2: (fast zero tester) (4 bonus points)

A standard n-bit zero tester, which outputs a one if the input consist only of zeros, uses an OR-tree as its core. It is interesting to note that there are technologies where NAND/NOR gates are faster than OR gates. Based on the equality

$$\overline{\overline{a \vee b \vee c \vee d}} = \overline{\overline{a \vee b} \wedge \overline{c \vee d}} = (a \text{ NOR } b) \text{ NAND } (c \text{ NOR } d)$$

the delay of the zero tester can therefore roughly be halved. Construct such a fast zero tester and provide formulae for its cost and delay. Use 2 as cost for OR/NOR/NAND, 1 as delay for NOR/NAND and 2 as delay for OR.

Exercise 3: (majority voter) (5 + 5 bonus points)

Let

$$n \in \mathbb{N},\ a \in \{0,1\}^{2 \cdot n+1},\ b \in \{0,1\}$$

For a given bit-vector a the function $major$ is defined as:

$$major(a) = \begin{cases} 1 & \text{if } (\sum_{i=0}^{2 \cdot n} a[i]) \geq (n+1) \\ 0 & \text{otherwise} \end{cases}$$

A *majority voter* is a circuit with inputs a and output b satisfying:

$$b = major(a)$$

In this exercise you need to construct a majority voter and prove the correctness of your construction.