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Department 6.2 - Computer Science
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Computer Architecture I - SS09

Exercise Sheet 7 (due: 29.06.09)

Exercise 1: (fast stall engine) (5 points)

The stall engine presented in the lecture has a linear delay of $O(n)$, where n is a number of stages. The reason for this is the following definition of the stall signal for a stage k (with $stall_n = 0$):

$$stall.k = full.k \wedge (hazard.k \vee stall.(k+1))$$

So, the signal $stall.1$ depends on all stall signals and has the obvious construction delay of $O(s)$.

In this exercise you are supposed to construct a stall engine, which computes the signal $stall.k$ for $k \in [1, n]$ with delay $O(\log(n))$.

Exercise 2: (exception predicates) (2 points)

In the lecture we introduced several types of interrupts. One of them is *illegal instruction*. Define and build hardware to test illegal instruction (as before use the instruction set given on the lecture's web page!).

Exercise 3: (DLX programming) (6 points)

Write a DLX assembler program that uses $\langle x[31:0] \rangle$ stored in GPR[4] and computes the value $\min(\{32\} \cup \{j | x[j] = 1\})$ and stores it in GPR[1]. The computation of this value must be no longer than $14 = 2 \cdot \lceil \log 33 \rceil + 2$. Comment your program in a way everyone can understand what it does.