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Computer Architecture I - SS09

Exercise Sheet 5 (due: 15.06.09)

Exercise 1: (delayed branch and delayed PC) (4 points)

In the lectures we mentioned Delayed Branch and Delayed PC mechanisms. In this easy exercise you are supposed to learn more about them (see Chapter 4 in the book S. Müller, W. Paul, Computer Architecture, Complexity and Correctness).

Prove the following theorem about the equivalence of Delayed Branch and Delayed PC: *Suppose a machine with delayed branch and a machine with delayed PC are started with the same program (without control operations in delay slots) and with the same input data. The two machines then perform exactly the same sequence* I_0, I_1, ... *of instructions.*

Exercise 2: (software conditions) (3 points)

In the lecture we defined the software conditions:

$$I_i \textit{ reads } gpr(x) \textit{ implies instructions } I_{i-1},\ I_{i-2},\ I_{i-3} \textit{ do not write to } gpr(x).$$

In this exercise you have to write this condition formally.

Exercise 3: (delay slot) (5 points)

Assume that we have a DLX machine with delayed branch and you as *compiler* for such a machine. In programmes for such a machine the delay slots should be filled either with NOP instructions (means: "no operation") or with some useful operations.

Take the program you wrote in the previous Exercise Sheet 4 (Exercise 3) (the correct version of the programm will be shown in the tutorial this week) and fill out the minimum of delay slots by NOP-operations. The smallest number of NOP-operations bring you the maximum amount of points.