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Computer Architecture I - SS09

Exercise Sheet 2 (due: 18.05.09)

Exercise 1: (cyclic left shifter) (2 points)

In the lecture we designed the n-cyclic left shifter. Let $n = 2^m$ be a power of two. The n-cyclic left shifter is a circuit with inputs $a[n-1:0]$, select inputs $b[m-1:0]$ and outputs $r[n-1:0]$ satisfying

$$r = cls(a, \langle b \rangle)$$

Prove the correctness of the n-cyclic left shifter by induction.

Exercise 2: (half decoder design) (2 + 2 points)

An n-half decoder is a circuit with inputs $x[n-1:0]$ and outputs $Y[2^n-1:0]$ such that

$$Y[2^n-1:0] = 0^{2^n-\langle x \rangle}1^{\langle x \rangle}$$

Construct the n-half decoder and prove its correctness by induction.

Exercise 3: (half decoder cost and delay) (2 + 2 points)

Assume that cost and delay of the gates AND, OR, and NOT are equal to one. Derive closed formulae (without recursion or $\sum$ symbols) for cost and delay for the n-half decoder. Prove the correctness of the derived formulae.

Exercise 4: (arithmetic right shift) (4 points)

In the lecture we defined the arithmetic right shift as follows

$$ars(a, i) = (a_{n-1}^i, a[n-1:i])$$

Prove or disprove the following statement

$$[ars(a, i)] = \left\lfloor \frac{[a]}{2^i} \right\rfloor,$$

where $\lfloor x \rfloor = k$ such that $k \in \mathbb{Z}$ and $(k \leq x) \wedge (x < k+1)$.