Saarland University
Department 6.2 - Computer Science
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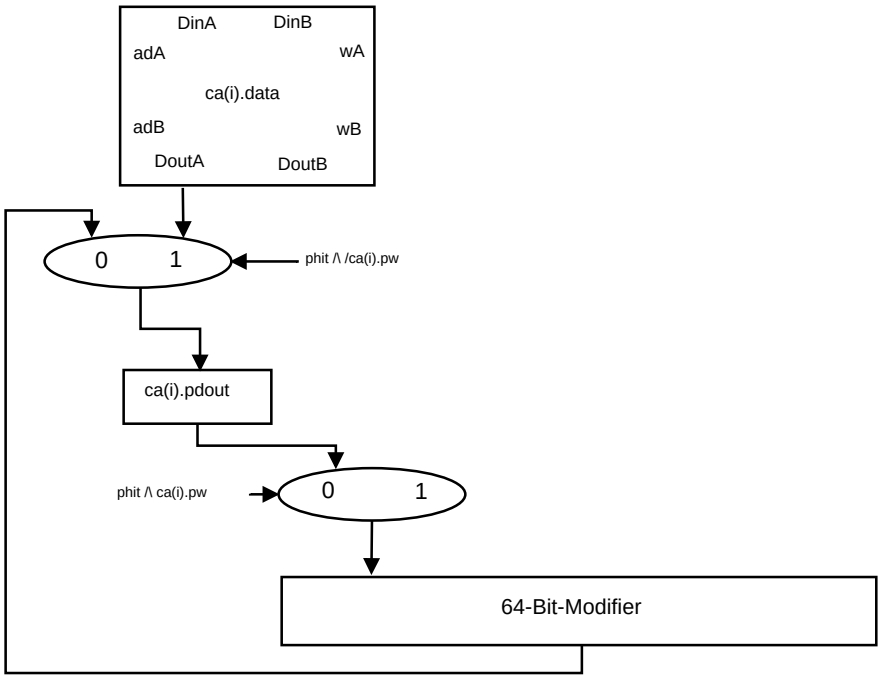
Multicore System Architecture - WS09/10

Exercise Sheet 8 (due: 15.12.09)

Exercise 1: (answers of reads) (4 points)

In the exercise you need to prove lemma "answers of reads". Note, that in order for the lemma to hold the following modification of the data paths for the Data-RAM of a cache is required.



Lemma(Answers of reads)
Let t be the last cycle of a read instruction, then *data* in cycle t is equal to the content of the abstract memory in cycle t at address a

$$t = e(i,j) \wedge /w(i,j) \longrightarrow (data(i,j) = aca(i).data(a)^{t+1}) \wedge (aca(i).s(a)^{t+1} \neq I),$$

where $a = ad(i,j)$.

Exercise 2: (test and set) (4 points)

Extend cache coherence theory so that we can use test and set instruction. Note, that in case of a read hit, when data is equal to 1, we need to finish the access in the same cycle as it starts (one cycle access).

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Exercise 3: (main theorem) (4 points)

In the lecture we have stated the two versions of the Main Theorem. In the exercise you need to prove (or at least to give a proof sketch) of any version of the Main Theorem.

The Main Theorem (ver.1): Let $access(i,j)$ be a read access, i.e. $/w(i,j)$, then it follows:

$$data(i,j)[b] = \begin{cases} data(last(ad(i,j),b,e(i,j)))[b] & \text{if } L(a,b,e(i,j)) \neq \emptyset \\ mm(ad(i,j))[b] & \text{otherwise} \end{cases}$$

The Main Theorem (ver.2): Let $access(i,j)$ be a read access, i.e. $/w(i,j)$, then it follows:

$$data(i,j)[b] = \begin{cases} data(\sigma^{-1}(last\sigma(a,b,\sigma(i,j))))[b] & \text{if } \exists z < \sigma(i,j).bw(\sigma^{-1}(z),a,b) \\ mm[b]^0 & \text{otherwise} \end{cases}$$