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Multicore System Architecture - WS09/10

Exercise Sheet 3 (due: 10.11.09)

Exercise 1: (coherence protocol) (4+4 points)

In the lecture we introduced master and slave diagrams for the cache coherence protocol. Explore the diagrams and explain what actions (including state transitions and bus signals) are performed by a master and a slave in case of

1. a read cache hit,
2. a write cache hit,
3. a read cache miss,
4. a write cache miss.

Answer the following questions:

1. In case of a write hit can it happen that data in the slave cache is in a shared state (O or S) and no slave cache hit occurs (CH signal equals 0)? Why?
2. In case of a read miss resulting states might violate the 4-th invariant (the protocol is not completely correct). How could we fix the problem? Would that require a change in the master control automaton construction presented on the lecture?
3. Are there any other violations of the 4-th invariant in the protocol?

You can find the tables describing the coherence protocol at the following url:
`http://www-wjp.cs.uni-sb.de/lehre/vorlesung/multicore_system_architecture/ws0910/layouts/signals.ppt`.

Exercise 2: (control automata) (4 points)

In the lecture we introduced a state diagram for the master and slave control automata implementing a coherence protocol from Exercise 1. The given protocol, however, is only one of the many possible coherence cache protocols. For example, we could change our protocol for the case of a write miss in such a way, that the master uses two consecutive transactions: to read the line (into states S, O, or E) and then modify it (entering O or M). In the exercise you need to provide the control automata for the modified protocol and describe master and slave protocol signals for the case of a write miss.